# A 25-kV 75-kHz Kicker for Measurement of Muon Lifetime

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***Abstract*—An international collaboration plans to measure the lifetime of the muon to a precision of 1 part per million [1]. The "MuLan" experiment will take place at the Paul Scherrer Institut (PSI) in Northern Switzerland. The MuLan experiment requires a fast beam line kicker, which can turn the beam on and off, to invoke an artificial time structure on the continuous beam which has a 50.6-MHz time microstructure. The kicker needs to run with a standard "on-off time cycle" or in a "Muon on Request" mode. The MuLan kicker consists of two pairs of deflector plates mechanically in series, driven by four modulators. Each modulator consists of two stacks of MOSFETs operating in push-pull mode. The specifications for the kicker demand that the rise and fall times of the deflector plate voltage do not exceed 45 ns. There is a requirement for an adjustable output voltage from 0 V to ±12.5 kV per deflector plate, a minimum pulse duration of 200 ns, and adjustable repetition rate up to a maximum of 50 kHz, continuous. Short turn-on and turn-off delays are required for the "Muon on Request" mode; the measured propagation delay is 200 ns. The specifications also require that the polarity of the pulses on the plates be selectable, although not on a pulse-by-pulse basis. This paper describes the novel design of the kicker and presents both predictions and measurements.**

***Index Terms*—Circuit simulation, electric fields, electrostatic devices, kicker, mesons, MOSFET power amplifiers, particle beam choppers, particle beam steering, power FET amplifiers, power FET switches, power FETs, power MOSFET switches, power MOSFETs, pulse generation.**

## I. Introduction

A FAST electric kicker is required to deflect a beam of surface muons and therefore invoke an artificial time structure on the continuous beam. The deflector plates are mounted horizontally and therefore the main component of the electric field between the deflector plates is vertical. Hence, the muon beam is deflected (kicked) vertically.

As a result of the current rating of commercially available fast MOSFETs the pulse rise time of 45 ns, for a ±12.5-kV deflector plate voltage, could not be achieved with one pair of 1.5-m-long plates and two modulators. Hence, the MuLan kicker consists of two pairs of deflector plates mechanically in series. A MOSFET-based modulator drives each deflector plate and therefore the two pairs of plates require four modulators. One plate of each pair is driven by a modulator to a maximum of $+12.5$ kV and the other plate of each pair is driven to a maximum of $-12.5$ kV. Therefore, the potential difference between a pair of deflector plates is variable up to 25 kV. Each pair of plates is 0.75 m long, 200 mm wide, and 5 mm thick, with a 2-mm radius on the edges, separated by 150 mm and housed in a beam pipe with an inside diameter of 600 mm. There is a virtual ground halfway between each pair of plates, which is a consequence of these plates being at equal voltage but opposite polarity. The two pairs of plates are separated longitudinally by 50 mm between the end of one pair and the start of the second pair.

The angle of deflection $(\theta_e)$, in radians, due to an electric field between the deflector plates, is given by

$$\theta_e = \arctan\left(\frac{V * \ell * c}{d * p * \beta * c}\right) \left[\frac{\mathrm{V}}{\mathrm{eV/c}}\right] \tag{1}$$

where $V$ is the potential difference between the deflector plates (adjustable up to 25 kV), $l$ is the overall length of the deflector plates (1.5 m), $d$ is the plate separation (0.15 m), $\beta * c$ is particle velocity, $c$ is the velocity of light in free space ($3 \times 10^8$ m/s), and $p$ is the beam momentum. From (1), a 30-MeV/c ($\beta = 0.28$) muon beam is deflected by 29 mrads, by a potential difference of 25 kV.

The code Opera3D [2] has been used to calculate the electric field between the deflector plates: these predictions can be used for beam tracking simulations. Fig. 1 shows the vertical component of the electric field, as a function of horizontal distance from the centerline of the deflector plates, halfway along one set of deflector plates, at two different vertical positions, for operation at ±12.5 kV. Parallel to the edge of the deflector plates the vertical field strength is approximately 75% of the nominal field strength (1667 V/cm).

In order to design the modulators, it is necessary to have a good knowledge of the total capacitance of the load. Equation (2) [3] gives a characteristic impedance $(Z)$ of the deflector plates of 56 Ω:

$$Z = 87 * \ln \frac{(5.98 * h/(0.8 * w + t))}{(\sqrt{\varepsilon r} + 1.41)} \tag{2}$$

where $h$ is the height above an infinite ground plane (75 mm), $w$ is the width of the deflector plates (200 mm), $t$ is the thickness of the deflector plate (5 mm), and $\varepsilon r$ (1) is the relative permittivity of the dielectric between the deflector plate and virtual ground plane.

A characteristic impedance of 56 Ω corresponds to a capacitance of 59.5 pF/m in free space, i.e., 44.6 pF per 0.75-m-long deflector plate. However, (2) neglects the presence of the beam

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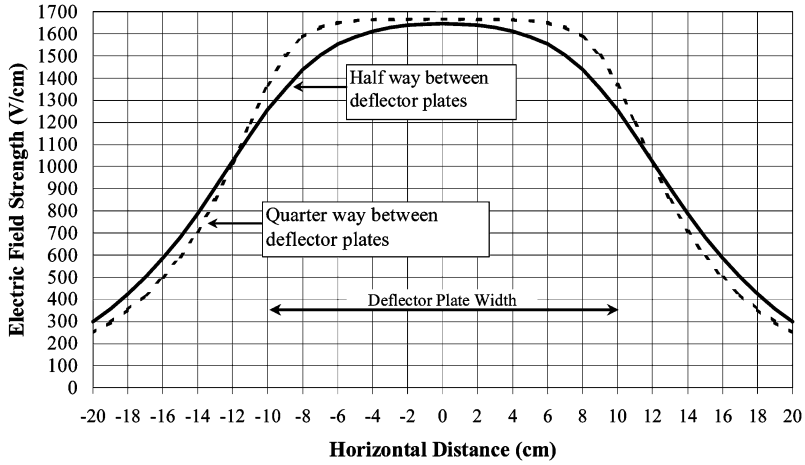


Fig. 1. Predicted vertical component of electric field, halfway along a set of deflector plates, at two different heights, for operation at ±12.5 kV.

pipe and insulating supports. A finite element analysis of one pair of deflector plates, the insulating supports and the beam pipe, using Opera3D [2], gives a predicted capacitance of 9.8 pF between deflector plates and approximately 26 pF from each deflector plate to the beam pipe. In the event that only one deflector plate, of a pair, is being operated and the second deflector plate is held at ground potential, then the total effective capacitance from the driven plate to ground is approximately 36 pF $(26\ \text{pF} + 9.8\ \text{pF})$. However, for the MuLan kicker, the two deflector plates of a pair are charged to opposite polarities, therefore there is a virtual ground halfway between the plates. Hence, under these circumstances, the effective capacitance to ground of each plate is approximately 46 pF $(26\ \text{pF} + 2 * 9.8\ \text{pF})$. Opera3D simulations show that an increase in the beam pipe inside diameter of 60 mm (10%) only reduces the capacitance of a 0.75-m-long deflector plate by 0.9 pF. A Fischer [4] DEE 107 A017-5 hermetically sealed high-voltage (HV) feed-through is used to connect from the output of each modulator to a deflector plate. An additional capacitance of 28 pF is expected as a result of the feed-through (25 pF), the connection to the modulator (2 pF), and the connection to a deflector plate (1 pF). Hence, there is an effective load capacitance of approximately 74 pF $(46\ \text{pF} + 28\ \text{pF})$ connected to the output of each modulator. Assuming an effective capacitance to ground of 10 pF for the stack that is turning on and 24 pF for an off-state stack of the modulator (Section III-E), a total capacitance of 108 pF must be charged to 12.5 kV in not more than 45 ns (10%–90% rise time definition), and subsequently discharged. Assuming an exponentially decaying charging and discharging current waveform, the maximum value of current limiting resistance is approximately 190 Ω per stack and the peak current is 66 A. The average current required from the HV power supply, to charge and discharge 108 pF, for operation at ±12.5 kV and 50 kHz (75 kHz) is 67 mA (101 mA) per modulator.

## II. Design Concept

The design of the modulators is based on previous designs at TRIUMF (Table I) [5]–[10] but incorporates significant modifications. For the design described in [10], the minimum pulsewidth is 350 ns; in addition the rise time is limited by the charge required to charge or discharge the deflector plates and the current rating of the MOSFETs. The latest design permits operation from dc up to more than 75 kHz at voltages of up to ±12.5 kV with an output load of approximately 80 pF.

TABLE I
Measured Values for TRIUMF Kicker Designs

| Pulse Voltage | Rise and fall Time | Repetition rate (continuous) | References |
|---|---|---|---|
| 6 kV | 30 ns | 10 Hz to 20 kHz | [5], [ 6] |
| 10 kV | 40 ns | 10 Hz to 1 MHz | [7], [8] |
| ±10 kV | 100 μs | <10 mHz to 10 Hz | [9] |
| −3.5 kV | 63 ns | DC to 52.2 kHz | [10] |
| ±12.5 kV | 40 ns | DC to 77 kHz | This paper |

The basic building block of previous TRIUMF modulators consisted of 1-kV modules that used an APT1004 [11] MOSFET. The APT1004 has a peak pulse current rating of 17.6 A [11], and is therefore not suitable for the present application without paralleling four or more APT1004s. A survey of power MOSFETs with voltage ratings of 1 kV and above resulted in the selection of the DE375-102N12A MOSFET from DEI [12] for the MuLan kicker; this choice was based upon the relatively high peak repetitive pulse current rating of 72 A combined with a relatively low gate charge (93 nC), short turn-on and turn-off delay times (5 ns), and fast turn-on (3 ns) and turn-off (8 ns) times. This DEI MOSFET is an RF avalanche rated device with a drain-source (D-S) rating of 1 kV and power rating of 220 W at a case temperature of 100 °C [12].

As a result of the relatively long maximum pulse length of previous designs (dc is possible for [9] and [10]), the HV output of the modulator for the TRIUMF designs is coupled directly to the deflector plates, and not via a pulse transformer. Instead, the gate and source of each MOSFET is electrically isolated from ground using a ferrite pulse transformer. The energy to turn on and turn off the APT1004 MOSFETs was magnetically coupled through the ferrite directly to the MOSFET gate-source (G-S). The primary side gate current waveform had a peak of 3 A: a fast rising edge was used to turn on or maintain in the on-state the APT1004 MOSFET and a fast falling edge was used to turn off or maintain in the off-state the APT1004 MOSFET [10]. Since the ferrite in each stack shared a common primary winding, the

turn-on and turn-off command was delivered almost simultaneously to each of the APT1004 MOSFETs.

The leakage inductance of the ferrite was acceptable with the gate charge ($\sim$35 nC) of the APT1004, although sets of parallel zener diodes were required to limit the maximum G-S voltage. The DE375-102N12A MOSFET has a gate charge almost three times greater than the APT1004. To switch the DEI MOSFET rapidly, in order to minimize both switching losses and the rise time of the current pulse into the deflector plates, a peak gate current of at least 12 A is required. A primary side gate current of 12 A, together with the leakage inductance of a ferrite pulse transformer, would require a relatively high power supply as well as significant protection to limit the maximum G-S voltage excursion of the MOSFET. Therefore, it was decided to use a MOSFET driver to directly drive each DEI MOSFET. After a survey of MOSFET drivers the DEIC420A low-side ultra-fast RF MOSFET driver was selected [12]. The choice was based on several features including its ability to sink and source high currents (20 A), minimum pulsewidth capability (8 ns), relatively short input to output delay time (32 ns), wide operating voltage range (8–30 V), and the compatibility of its package with the DE375-102N12A MOSFET.

Several ways of deriving the energy for the MOSFET driver were considered, including tapping of energy from the D-S of the MOSFET: this method was discarded as it is not conducive to output pulses which result in 0-V D-S for an extended time, e.g., dc operation. Instead, a ferrite is used to magnetically couple energy to a G-S power supply.

Various options for gating the MOSFET driver on and off were considered, including the following:

1) magnetically coupling the trigger signal through the power supply ferrite and use a "masking circuit" to discriminate the trigger pulse from the charging current;
2) using a second ferrite to magnetically couple the trigger signal;
3) using fiber optics for the trigger signal.

Initial research into various "masking circuits" was not fruitful. A second ferrite would need to be reasonably large in order to achieve the required voltage isolation and to minimize parasitic capacitance from the source of each MOSFET to the primary winding. Three-dimensional (3-D) electromagnetic simulations show that the presence of a second ferrite, with dimensions 2.4-in outside diameter, 1.2-in inside diameter and 0.5-in high, would increase the parasitic capacitance to ground by 0.8 pF per module. Therefore, a fiber optic system was selected to provide the turn-on and turn-off trigger signal to the MOSFET driver. The HFBR-2528 fiber optic receiver from Agilent [13] was chosen. This receiver provides a CMOS/TTL output (and is therefore directly compatible with the TTL input of the DEI MOSFET driver) and is specified over an operating range from dc to 10 MBd [13]. The dc rating is important as it minimizes the susceptibility to erratic switching due to noise. The receiver is sensitive to electric fields and is hence covered with a copper shield (Fig. 3).

## III. Circuit Design and Control

The design of the modulators is based on previous designs at TRIUMF (Table I) [5]–[10] but incorporates significant modifications. For the design described in [10], the minimum pulsewidth is 350 ns; in addition, the rise time is limited by the charge required to charge or discharge the deflector plates and the current rating of the APT1004 MOSFET. The latest design permits operation from dc up to more than 75 kHz at voltages of up to $\pm$12.5 kV with an output load of approximately 80 pF.

### A. Introduction

A MuLan modulator consists of two stacks of 17 1-kV modules per stack, operating in "push-pull" mode; when one stack is on, the other stack is off. There are a total of 136 1-kV modules for the four modulators. One stack is referred to as the "pull down" (PDN) stack and the other is referred to as the "pull up" (PUP) stack. For a positive output pulse, a "pull up" stack charges one deflector plate to high voltage and subsequently the corresponding "pull down" stack discharges the deflector plate to ground. For a negative output pulse, a "pull down" stack charges one deflector plate to high voltage and subsequently the corresponding "pull up" stack discharges the deflector plate to ground. The 1-kV modules plug into a backplane.

### B. Module

Fig. 2 shows an electrical schematic of a 1-kV module. The maximum G-S voltage rating of the DE375-102N12A is $\pm$20 V continuous ($\pm$30 V transient) [12]. The propagation delay of the DEIC420A MOSFET driver is dependent upon both input voltage and supply voltage. A supply voltage of 16 V has been chosen as it results in the specified propagation delay (32 ns), with an input voltage of 5 V, while providing an operating margin to the 20-V continuous rating of the G-S of the DEI MOSFET. The total effective output capacitance of the DEIC420A and input capacitance of the DE375-102N12A MOSFET has been measured to be 11 nF with 0-V D-S.

A full-wave rectifier, consisting of four fast high-current ES1B diodes [14], connected across a two-turn secondary on the ferrite, together with approximately 4 $\mu$F of surface mount capacitors, provides the dc power supply for the DEIC420A driver (Fig. 2). These capacitors range from size 1206 and value 0.01 $\mu$F (C1, C2, C4, C6, C7, C9), to size 1210 and value 0.47 $\mu$F (C3, C5, C8, C10), to size 1210 and value 2.2 $\mu$F (C13). The surface mount capacitors are used for the dc power supply and provide a low-inductance path for the pulse current supplied to the gate of the MOSFET. A size 1206 surface mount capacitor (3.2 mm long and 1.6 mm wide) has a parasitic inductance of approximately 1.2 nH [15]; the parasitic inductance of a size 1210 capacitor (3.2 mm long and 2.5 mm wide) would be expected to be less than that of the size 1206.

Capacitor C13 is connected directly across the output of the bridge rectifier and, together with the bridge rectifier, provides 16-V dc power. The supply voltage for the HFBR-2528 fiber optic receiver is derived from the 16-V dc power supply using a 220-$\Omega$ resistor (Rfo) and a 5.1-V zener (Zfo) with a tolerance of $\pm$2%. A zener diode proved to be a more reliable option, in a noisy environment, than a voltage regulator. The dc supply current drawn by the fiber optic receiver is measured to be in the range of 25–35 mA, and the current through the 5.1-V zener is approximately 20 mA.

The DE375-102N12A MOSFETs and DEIC420A MOSFET drivers are capable of maximum switching frequencies of 50 and

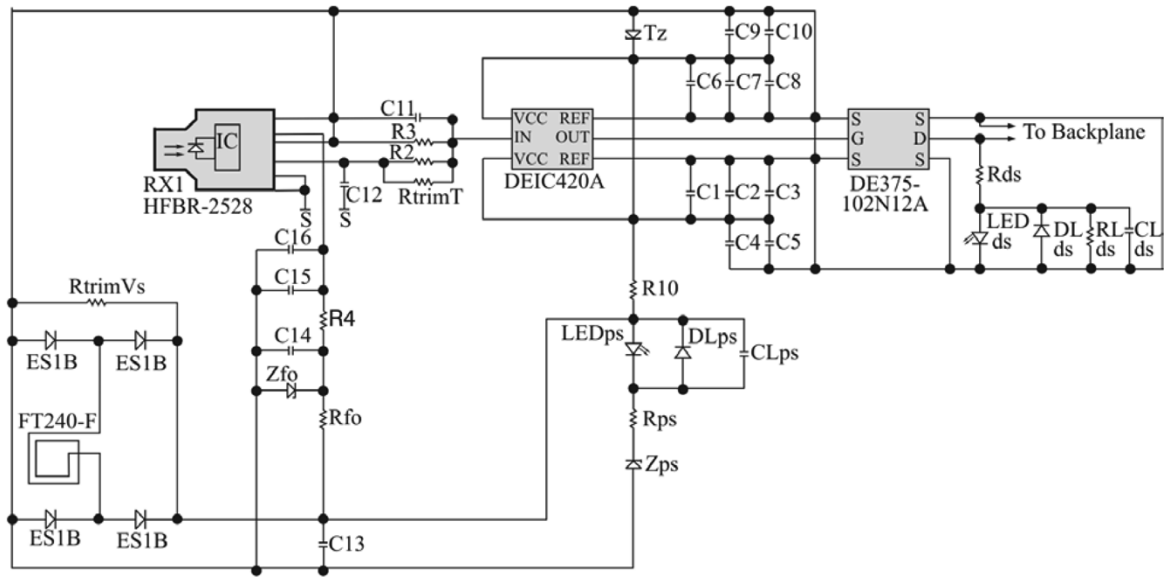


Fig. 2. Electrical schematic of a 1-kV module.

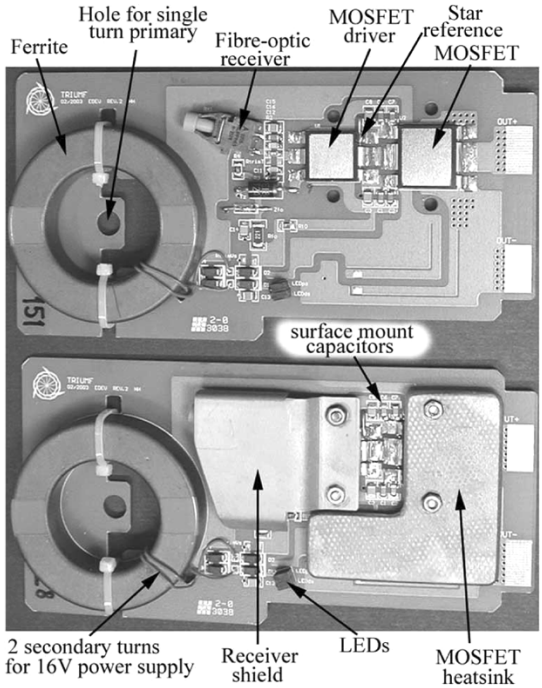


Fig. 3. Topside of 1-kV modules.

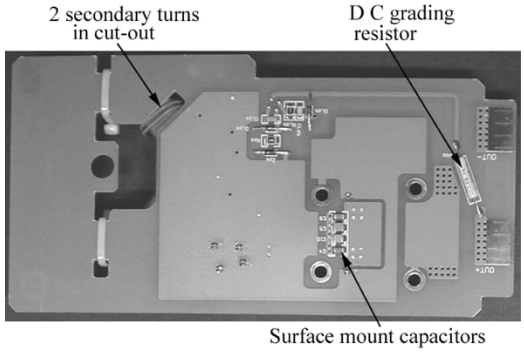


Fig. 4. Underside of a 1-kV module.

45 MHz, respectively [12]. A limit on the maximum frequency of operation of the 1-kV modules is imposed by the HFBR-2528 fiber optic receiver, which is rated at 10 MBd [13], otherwise the basic design of modules is limited by power dissipation and has operated reliably at 3.5 MHz (Section VI).

The layout of the circuit for the 1-kV modules required careful analysis with special consideration of the high current paths for both the MOSFET D-S current and the charge-discharge current provided, by the DEIC420A driver, to the G-S of the DEI MOSFET. A star reference point for the 16-V dc supply, fiber optic receiver, and MOSFET driver, is at the top of one of the output legs of the MOSFET driver (Fig. 3). This reference point is chosen as it minimizes the effect of transients, which result from a high rate-of-change of output current of the MOSFET driver, upon the fiber optic receiver. Surface mount capacitors, carefully laid out on both the topside of the PCBs (Fig. 3), and on the underside (Fig. 4), provide low-inductance paths for the G-S current for the MOSFET.

Each module has a dc grading resistor of 1.6 MΩ±1% (Rds); a high-efficiency red LED (type HLMP-Q155-F0010 [13]) provides a diagnostic for the D-S voltage. The red LED is on provided that the D-S is supporting high voltage, but goes out if there is no HV D-S (e.g., due to the MOSFET being on or having failed to short-circuit). A high-efficiency yellow LED (type HLMP-7019-D0010 [13]), in series with a 12-V±2% zener (Zps) and an 806-Ω resistor (Rps), provides a diagnostic for the 16-V dc power supply on each module. An 18-V±5% tranzorb (Tz), type 1V5KE18A [14], limits the low-voltage dc power supply voltage to a safe level for the components.

The energy magnetically coupled onto each 1-kV module is provided via a single-turn primary through a FT240-F ferrite [16] (Fig. 3); the ferrite dimensions are 2.4-in outside diameter, 1.2-in inside diameter and 0.5-in high. The primary circuit is described in Section III-H.

The MOSFET is sandwiched between the PCB and a copper heat sink to give double-sided cooling. The copper heat sink is

3.2 mm thick and does not have any fins: this permits the spacing between adjacent modules to be minimized (Section III-D). The surface area of the topside of the heat sink is approximately 24.6 $cm^2$. Calorific measurements, in ambient air, give a thermal impedance, from heat sink to air, at a heat sink temperature of 90 °C, of approximately 9 °C/W. With fans producing a flow rate of about 1 m/s (200 feet/min), over the heat sink, the thermal impedance, from heat sink to air, at a heat sink temperature of 90 °C, is approximately 3 °C/W. The data sheet value of the thermal impedance from junction to case, for the DE375-102N12A MOSFET, is 0.16 °C/W [12].

Red-X corona dope is applied on the sides of the drain leg and output source legs of the DE375-102N12A MOSFET in order to help prevent corona: the datasheet value for dielectric strength of the corona dope is 3.8 kV/mil [17]. In addition, the heat sink, which has rounded edges, is sized such that it acts as an equipotential plane above the MOSFET (Fig. 3). To prevent induced current loops, the heat sink is connected to source potential via only one of the mounting screws.

Various types of Amidon ferrite [16] have previously been evaluated for the pulse transformer to determine the best type for directly providing the gate pulse to the MOSFET [10]. However, in the latest design the ferrite transformer does not directly provide the gate drive to the MOSFET; instead, there is an intermediate MOSFET driver. Hence, a number of types of ferrite cores have been evaluated for the pulse transformer for the MuLan kicker, to determine the best type for achieving a high-efficiency power supply with a pulsed primary. The materials evaluated include types 43, 61, 67, 77, F, J, K, and W from Amidon [16]. All the ferrite cores from Amidon were evaluated in size FT240 (2.4-in outside diameter, 1.2-in inside diameter, 0.5-in high). The Amidon cores range from low permeability ($\mu_r = 40$ for material 67), to medium permeability ($\mu_r = 850$ for material 43), to high permeability ($\mu_r = 10\,000$ for material W). All these ferrite types were initially measured, with an open circuit secondary, on an LCR bridge and types 61, 67, K, and W were discounted because of their low magnetizing inductance and high core losses at 1-MHz ac. Ferrite types 43, 77, and F were tested with a pulse current on their primary, and with a full bridge rectifier, filter capacitor, and representative dc load on the secondary. The primary voltage was set to 19-V dc in series with a 4.2-$\Omega$ resistor; the pulsewidth of the primary current and number of secondary turns were varied for each of the three-ferrite types. A single-turn primary was used, as this greatly simplifies the mechanical arrangement of the modulators as well as helping to minimize the parasitic capacitance from each module to the primary winding. The 19-V was chosen as this scales to 325 V for 17 series cards, which is a convenient voltage magnitude.

The average secondary current drawn is dependent upon the frequency of operation of the MOSFETs, and varies from approximately ~50 mA for dc operation, to ~60 mA at 50 kHz, to ~220 mA at 1 MHz, to ~570 mA at 3 MHz. If necessary, the frequency of the primary pulse can readily be altered via the controls circuit to provide the required secondary current. The type F ferrite proved to be the most efficient of the ferrites tested, and gave a very linear relationship between the frequency of the primary pulse required, to maintain 16-V dc on the secondary, and the secondary load current. As a result of the leakage inductance of an FT240-F ferrite (~100 nH at 1 MHz), and the parasitic inductance of the primary winding, exciting the primary current for less than approximately 400 ns does not result in efficient transfer of energy to the secondary. Similarly increasing the primary current pulsewidth beyond 1 $\mu$s results in a higher than necessary average primary current. Therefore, a primary current pulsewidth of 1 $\mu$s has been chosen.

A linear PSpice model of the FT240-F ferrite, which results in waveforms similar to those measured, has a magnetizing inductance and equivalent core loss resistance of 9 $\mu$H and 30 $\Omega$, respectively.

### C. Main Current Loop

Two HCK 1600-12500 [18] high-voltage capacitor-charging power supplies, one for providing energy to the two positive deflector plates and one for providing energy to the two negative deflector plates, are used. The output from each HV power supply is via a coaxial cable (type LEMO 130660, rated at a maximum voltage of 30 kV [19]); this coaxial cable is wound on a G10 former to create an air-cored inductor with a value of approximately 10 $\mu$H. This inductor acts as a filter to common mode current. The output from the inductor connects, via a Ross Relay [20] (Section III-G) and filter resistor to a 60-nF high-voltage smoothing capacitor. This capacitor provides the pulse current for charging the deflector plates. The pulse current flows from the 60-nF capacitor, through current-limiting resistors (Section III-F), and through the D-S of the stack of MOSFETs that are turning on, to the deflector plates. The return current flows through an insulated cable back to the groundside of the 60-nF capacitor. The partial inductances of the main current loop have been calculated using FastHenry [21]. For simulation purposes, the current loop has been approximated as a rectangle with a width of 240 mm and a height of 600 mm. FastHenry gives a total inductance of 1.68 $\mu$H for a conductor with a square cross section of 2.5 mm by 2.5 mm. The breakdown of this inductance is:

- 717-nH self inductance for each 600-mm-long side;
- 243-nH self inductance for each 240-mm-long side;
- Mutual inductance of −111 nH from one 600-mm side to the other;
- Mutual inductance of −9 nH from one 240-mm side to the other.

The combination of the self and mutual inductances, for each side of the rectangular current path, corresponds to an inductance of approximately 1 nH/mm.

The main current path through the stack of 1-kV modules actually zigzags from side to side and from the backplane forward to the drain or source of each MOSFET. After the system was built the inductance of five series modules was measured, at a frequency of 1 MHz, between the drain of one module and the drain of a module 10 cm below; to do this, the MOSFETs were held in the on-state. The measured inductance corresponds to 60 nH per module: based on the 1 nH/mm, the inductance due to the vertical separation (20 mm) between centers of adjacent modules is 20 nH, and therefore the inductance due to the zigzag path, MOSFET, and a backplane connector is 40 nH per module.

### D. Parasitic Capacitance and Transient Voltage Grading

Each modulator for the MuLan kicker is housed in a metal cabinet. To obtain a compact design with relatively low parasitic capacitance, the dimensions and separation between modules are kept to a practical minimum. The overall length of each PCB module is 164 mm and the maximum width is 84 mm. The MOSFET is sandwiched between the PCB and a copper heat sink to give double-sided cooling. The copper heat sink is 3.2 mm thick. The total thickness of the PCB, MOSFET, heat sink, and mounting hardware is 12 mm: this is intentionally less than the total thickness (15.2 mm) of PCB (1.5 mm), ferrite (12.7 mm), and the two secondary turns (1 mm) on the top of the ferrite. The two secondary turns on the underside of the board lie in a "cut-out" of the PCB so that they do not further increase the height of the module (Fig. 4). A module spacing, measured between centers of the PCB, of 20 mm has been chosen; this gives a minimum clearance of 4.8 mm between adjacent modules in a stack. High-voltage breakdown tests were carried out on the previous generation of these modules. These spare modules had been sitting in the laboratory for a number of years and were dusty. The weather was cold and dry for the breakdown tests. A distance of 20 mm between centers separated the PCBs and the closest point between modules (heat sink screws) was 2.3 mm. The HV was gradually turned up until breakdown occurred. Breakdown occurred at approximately 5.5 kV, i.e., 2.4 kV/mm, in ambient air. This breakdown voltage was virtually independent of polarity. Hence, a minimum clearance of 4.8 mm between PCB centers, for the MuLan kicker, gives a conservative and reliable design for a maximum of 1 kV between adjacent modules.

The parasitic capacitance to ground from each module significantly affects transient voltage grading down the stack of modules. Analytical equations have been derived to calculate the approximate variation in voltage per module as a function of the capacitance ratio $k$ [5]:

$$k \cong \left(\frac{C_{gnd}}{C_{m(n)}}\right) \tag{3}$$

where $C_{gnd}$ is a parasitic capacitance to ground of one module, averaged for all modules in a stack, and $C_{m(n)}$ is the total linearized drain-to-source capacitance of a 1-kV MOSFET in module number $n$, including parallel grading capacitance. If $k$ is small then the variation in voltage per module [5] is given by

$$V_{m(n)} \cong V_{m(1)}\left(1+\sum_{i=1}^{n-1} ik\right) \tag{4}$$

where $V_{m(n)}$ is the transient voltage across module number $n$, and $V_{m(1)}$ is the transient voltage across module number 1. Module 1 is closest to the dc end of the stack (i.e., high voltage power supply or ground end), and module $n$ is closest to the pulse deck.

Connecting a fast-grading capacitor between the drain and source of the MOSFETs can minimize the severity of the voltage transient across a module. Most of the parasitic capacitance to ground of a module is associated with the source of the MOSFET; this is as a result of the majority of the module being at source potential. The source of the module at the pulse end of the pull up stack is on the pulse deck whereas, in the pull down stack, the drain of the module at the pulse end of the stack is on the pulse deck. Hence, the ideal value of fast-grading capacitor is dependent upon whether the pull up or pull down stack is being considered. Equation (5) gives the values of fast-grading capacitors that would result in ideal voltage distribution in the pull up stack:

$$C_{fgUp(n)} = \sum_{i=1}^{n-1} i * C_{gnd(i)} \tag{5}$$

where $C_{fgUp(n)}$ is the value of the fast-grading capacitor required to be connected between the drain and source of the MOSFET of module $n$ of the pull up stack, and $C_{gnd(i)}$ is the parasitic capacitance to ground of module $i$. No fast-grading capacitor is connected across module 1.

Equation (6) gives the values of fast-grading capacitors that would result in ideal voltage distribution in the pull down stack.

$$C_{fgDn(n)} = \sum_{i=2}^{n} (i-1) * C_{gnd(i)} \tag{6}$$

where $C_{fgDn(n)}$ is the value of the fast-grading capacitor required to be connected between the drain and source of the MOSFET of module $n$ of the pull down stack.

Fig. 2 shows an electrical schematic of a 1-kV module. The values of the fast-grading capacitors (not shown in Fig. 2) are dependent upon the position in the stack [see (5) and (6)]; hence, to ensure that the modules can be interchanged, the fast-grading capacitors are connected on the back plane. A 110-$\Omega$ resistor is connected in series with each fast-grading capacitor to limit discharge current at turn-on of the MOSFETs. At the pulse end of the stack, the fast-grading resistors dissipate approximately 10 W each at 75 kHz. These resistors, noninductive ceramic composite resistors type R1010T111J from HVR [22], are mounted in a G10 structure beside the stack of modules (Fig. 5). The overall width of the modules, lexan support frame, and fast-grading resistors with G10 support frame, is 137 mm.

Opera3D has been used to determine the parasitic capacitance to ground of the modules together with fast-grading resistors. The simulations modeled each module as an equipotential "brick" with a height of 15 mm, and a separation of 20 mm between centers. The model included a ground conductor, 8 mm in diameter, to represent the inner conductor and insulation of the inner conductor of the HV coax cable, type HTC-50-7-2 rated at 18 kV [23], used for the single-turn primary of the ferrite transformer. In the stacks, the return conductor of this coax is removed before the cable is installed through the ferrite. The average of the predicted capacitances, of 1.7 pF per module, is attributable to both the capacitance to the metal cabinet ($\sim$1 pF per module) and the capacitance to the primary winding of the ferrite transformer ($\sim$0.7 pF) [24]. The predicted capacitances range from 1.6 to 1.8 pF per module for the central 13 modules of a stack, to 2 pF per module for the second and 16th modules, to 4.7 pF per module for the end modules.

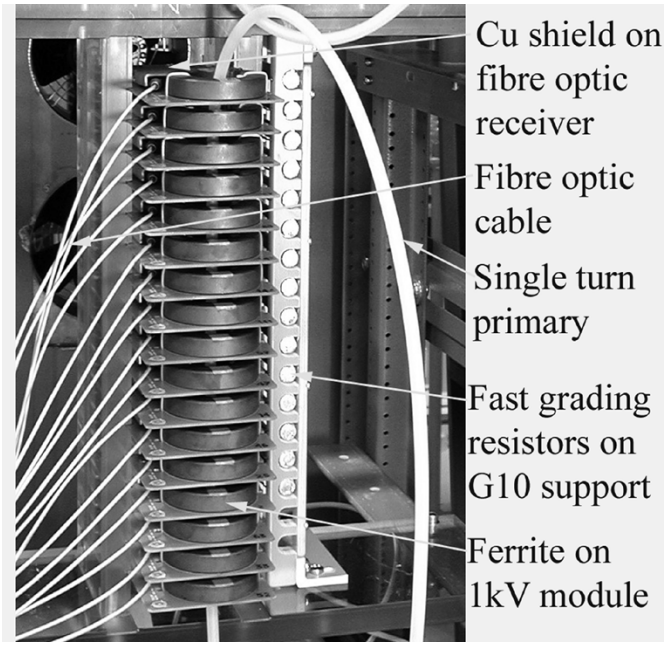


Fig. 5. Pull down stack of 17 1-kV modules.

### E. Effective Capacitance of Stacks

Each modulator consists of two stacks operating in push-pull (Section III-A). One stack turns off and subsequently the other stack turns-on (Section III-I). The stack turning-on carries the current which charges up the capacitance of the following:

1) output load (Section III-C);
2) off-state stack;
3) parasitic capacitances to ground of the stack turning-on.

*Off-State Stack:* The voltage-dependent incremental capacitance $(C_{\text{incremental}})$ of a DE375-102N12A MOSFET has been measured (Fig. 6); the parameters of a PSpice [25] MOSFET model have been adjusted to closely reproduce the measured incremental capacitance. Fig. 6 also shows the linearized effective capacitance $(C_{\text{effective}})$ of the MOSFET; this is calculated from stored energy using (7)

$$C_{\text{effective}} = \left(\frac{2}{V_i^2}\right)\left(\int_0^{V_i}\left(\int C_{\text{incremental}} \cdot dV\right) dV\right) \quad (7)$$

where $V_i$ is the drain-source voltage of interest.

A DE375-102N12A MOSFET operated at 750 V has a linearized effective capacitance of approximately 150 pF (Fig. 6).

An analysis of the effective capacitance of an off-state stack to ground, with a parasitic capacitance of 0.7, 1.7, or 2.7 pF per module, has been carried out (Fig. 7). The effective capacitance $(= (2{*}E/V^2))$ to ground of an off-state stack is calculated from the energy $E$ required to charge the capacitance of this stack to voltage $V$. Most of the parasitic capacitance to ground of a module is associated with the source of the MOSFET; this is as a result of the majority of the module being at source potential. The source of the module at the pulse end of the pull up stack is on the pulse deck whereas, in the pull down stack, the drain of the module at the pulse end of the stack is on the pulse deck; hence, the effective capacitance to ground is different for the pull up and pull down stacks.

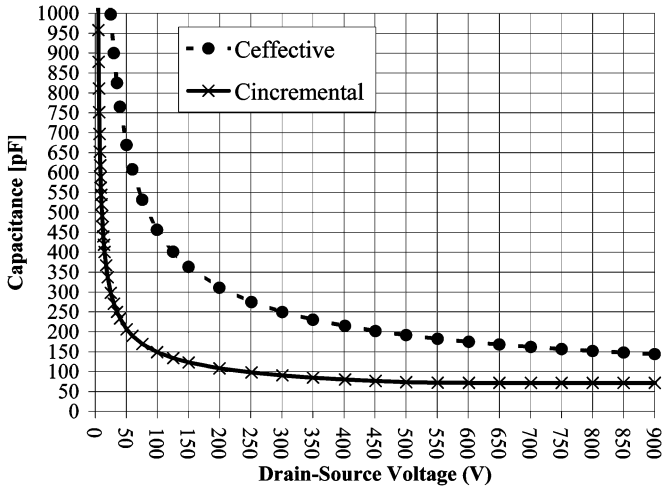


Fig. 6. Measured voltage-dependent incremental capacitance $(C_{\text{incremental}})$ and effective capacitance $(C_{\text{effective}})$ of a DE375-102N12A MOSFET.

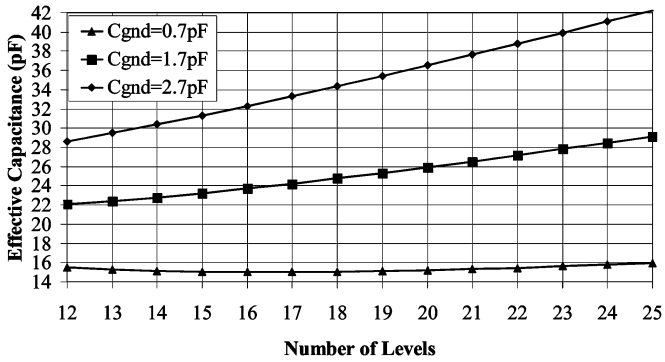


Fig. 7. Effective capacitance to ground of an off state pull up stack of DE375-102N12A MOSFETs (12.5 kV per stack) with fast-grading capacitors.

The analysis of the effective capacitance, presented here for the pull up stack, includes the incremental capacitance of the DE375-102N12A MOSFET as well as ideal values of fast-grading capacitors calculated from (5). From (5), with a parasitic capacitance to ground of 1.7 pF per module (Section III-D), the 17th module, which is at the pulse end of the stack, would require a fast-grading capacitance value of 231 pF.

As a result of the voltage dependence of the incremental capacitance of the MOSFET, the equivalent linearized capacitance of an off-state stack, which would result in the predicted 10% to 90% rise time, is between 13% less (for 12 series modules) to 6% less (for 24 series modules) than the effective capacitance of the stack.

When the parasitic capacitance to ground is small (e.g., 0.7 pF per module or less) the effective capacitance is a minimum with 16 series modules. With a larger parasitic capacitance to ground, e.g., 1.7 pF per module, the effective capacitance approaches a minimum $(\sim$22 pF) with 12 series modules. However, with only 12 series modules, the DE375-102N12A MOSFETs would be operating above their maximum D-S voltage rating of 1 kV. Seventeen modules per stack results in an effective capacitance of 24 pF, for the off-state pull up stack, but permits the design to be used at up to 12.5-kV output voltage, resulting in a nominal

voltage of 735 V per module, therefore providing some redundancy of the modules. The corresponding effective capacitance for the 17 modules of the pull down stack is 22.3 pF.

*Stack Turning-On:* The dc grading resistors (Section III-B) have a tolerance of $\pm 1\%$ and result in good dc voltage grading in an off-state stack. Therefore, just prior to turn-on of the pull up stack, the dc voltage is assumed to be graded linearly, e.g., from full dc voltage at the dc end of the stack to 0 V at the pulse end of the stack. At turn-on of the pull up stack, the parasitic capacitance to ground of 1.7 pF per module (Section III-D) must be charged to the full dc voltage. Hence, the voltage associated with the 1.7 pF of module number 17, at the pulse end of the pull up stack, must swing through the full voltage, whereas the voltage associated with the 1.7 pF of module number $i$ must swing through $(i/17)^{\text{th}}$ of the dc voltage.

The equivalent parasitic capacitance to ground, of the stack turning on, has been derived based on a consideration of the energy required to charge the parasitic capacitances. The source of the module at the pulse end of the pull up stack is on the pulse deck whereas, in the pull down stack, the drain of the module at the pulse end of the stack is on the pulse deck. Hence, the equivalent parasitic capacitance to ground is dependent upon whether the pull up or pull down stack is being considered. For the pull up stack, the equivalent parasitic capacitance to ground $(C_{eq\text{-}gndUp})$ is given by

$$C_{eq\text{-}gndUp} = \sum_{i=1}^{17} \left(\frac{i}{17}\right)^2 * C_{gnd(i)}. \tag{8}$$

For the pull down stack, the equivalent parasitic capacitance to ground $C_{eq\text{-}gndDn}$ is given by

$$C_{eq\text{-}gndDn} = \sum_{i=1}^{17} \left(\frac{i-1}{17}\right)^2 * C_{gnd(i)}. \tag{9}$$

For a parasitic capacitance to ground of 1.7 pF per module, from (8), the equivalent capacitance to ground for the pull up stack turning-on is 10.5 pF. The pull up stack also drives the 22.5-pF capacitance of the off-state pull down stack (see above), i.e., a total capacitance of 33 pF for the two stacks. From (9), the equivalent capacitance to ground for the pull down stack turning-on is 8.8 pF; this stack also drives the 24-pF capacitance of the off-state pull up stack (see above), i.e., a total capacitance of 32.8 pF for the two stacks. Hence, the total capacitance of the off-state stack and stack turning-on is approximately 33 pF, irrespective of the stack being considered.

### *F. Current Limiting Resistance*

Resistors are used to limit the maximum current, through the DEI MOSFETs, to a safe magnitude, during both normal and fault conditions. The DE375-102N12A MOSFETs are rated at 72 A pulsed. Therefore, for operation at $\pm 12.5$ kV a resistance of 174 $\Omega$ is required to limit the current to a maximum of 72 A. The on-state resistance of the DE375-102N12A MOSFETs has been measured to be approximately 1 $\Omega$ at 30 °C and 2 $\Omega$ at 120 °C junction temperature. Therefore, with 17 series modules, an additional 157 $\Omega$ of resistance is required to limit the D-S current to 72 A at 30 °C.

In previous designs of modulators at TRIUMF [5]–[10], the current limiting resistance was distributed throughout each stack of MOSFETs. This has the advantage that the distributed resistors help to minimize the effect of discharge of local parasitic capacitance. However, for the MuLan kicker design, in order to be able to easily cool the resistors and also to minimize the parasitic capacitance to ground of each module, the current-limiting resistance is lumped at the dc end of the stack. This method of implementing the current-limiting resistance has the disadvantage that, at turn-on of the modules in a stack, there is a large voltage transient at the dc end of the stack. This voltage transient is due to the presence of the current limiting resistance (both its resistance value and parasitic inductance) between the 60-nF smoothing capacitor (Section III-C) and the dc end of the stacks. The voltage transient may potentially cause significant electric noise problems, e.g., because the local parasitic capacitances can charge or discharge rapidly.

The current-limiting resistors employed for each stack in the MuLan kicker are 2 series, 18-in-long 1-in-diameter noninductive bulk ceramic resistors, type 890SP rated at 375 W each, from Kanthal Globar [26]. The resistance values were measured and selected in pairs to give 167 $\Omega$. These resistors have a positive temperature coefficient of approximately 0.06%/°C.

### *G. Selection of Output Polarity*

One, two pole, double throw HV Ross Relay [20], per HV power supply, is used to automatically reconfigure the circuit of the modulators, depending on the polarity of output pulse selected. The polarity is selected on the front panel of the HV power supply; the supply must first be de-energized to prevent internal damage. The voltage reversal switch, on the HV power supply, is situated behind the front cabinet door. Hence, the door must be opened to access the voltage reversal switch. Microswitches on the doors trip the power supplies in the event that a door is opened while the power supplies are still turned-on. The polarity read back is also fed to the controls (Section III-I).

### *H. Primary Side Circuit*

The energy magnetically coupled onto each 1-kV module, for the 16-V dc power supply, is provided via a single-turn primary through a FT240-F ferrite (Section III-B). The primary pulse current is approximately 2.2-A magnitude, with fast rise and fall times. Each stack of 17 modules has its own primary winding (Fig. 5), hence, a total of eight primary windings are required for the MuLan kicker. The current in each primary winding is derived from charge storage capacitors, a series 85-$\Omega$ resistor type G01KGA850J [22], and a primary side driver module. A DE375-102N12A MOSFET, in each primary side driver module, generates the current pulses at a repetition rate of 90 kHz with a pulsewidth of 1 $\mu$s. An MCN 700-350, 350 V, power supply [18], rated at 2 A, supplies the average primary current for all eight stacks of the four modulators.

The layout of the electrical circuit of a primary side driver module is very similar to that of the 1-kV modules in the stacks. However, each primary side driver module has the following additional circuitry.

- 220 pF in series with 110-$\Omega$ (10-W) connected drain-source across the DE375-102N12A MOSFET,

to attenuate the voltage transient which occurs when the MOSFET turns-off the 2.2 A of current flowing through the inductance associated with the primary of the 17 ferrite transformers. The 110-Ω resistor dissipates approximately 6 W. When the 1-kV modules in a stack turn on, the source of each of the MOSFETs of these modules changes in voltage rapidly. PSpice simulations, for operation of a modulator at 12.5 kV, show that the rapid change in source voltage, together with the parasitic capacitance between the primary and secondary of the ferrite pulse transformer of each module (Section III-D), results in a peak current of 8 A being injected into the primary winding. Two watts of the 6-W dissipation, in the 110-Ω of a primary side driver module, is attributable to the capacitive coupling of the source voltage transients to the primary winding.

- Two series-connected 110-V tranzorbs, connected in series with a total resistance of 8.2-kΩ and an HFBR-1523 [13] high-efficiency fiber optic transmitter. This circuit is connected across the input 315-V power supply rails to provide an interlock (see below).

The primary side driver modules do not have a ferrite to provide the low-voltage dc power for the fiber optic receiver and MOSFET driver; instead, a 12-V dc floating power supply is used to supply the two primary side driver modules in each modulator. To ensure that the two primary side driver modules in each modulator are electrically floating with respect to the controls board, a second independent dc power supply is used for the controls and interlocks. For operation at 12-V, the value of the resistor Rfo (Fig. 2), of a primary side driver module, is reduced to 150 Ω, and the zener voltage of Zps is reduced to 8 V$\pm$5%.

During tests on prototype 1-kV modules, for the MOSFET stacks, a potential problem was noticed; if the 16-V power supply ramped up to slowly, feedback between the HFBR-2528 fiber optic receiver and MOSFET driver resulted in a very high-frequency oscillation. This oscillation loaded down the power supply and therefore prevented the voltage rising up to 16 V. This could also happen if the 90-kHz current pulse through the primary of the ferrite transformers were present as the output of the 350-V power supply ramped up. In order to prevent this latch-up, controls and interlocks ensure that the output of the 350-V power supply is above approximately 85% of its normal operating value of 305 V before the MOSFET of each primary side driver module is gated on and off. This is achieved by selecting the tranzorb voltage rating and resistance value, in conjunction with the HFBR-1523 transmitter characteristics (see above), to give appreciable light output of the transmitter at 260 V. The output of the HFBR-1523 is used as a gate on the controls board (Section III-I) for the 90-kHz command signal for the primary side driver modules.

### *I. Controls and Interlocks*

At PSI, the four racks of the MuLan kicker are each provided with synchronized TTL signals for turning the kickers on and off. The convention chosen for the TTL signal is that a 0-V input corresponds to 0-V output on a deflector plate. A high input corresponds to a high output of up to $\pm$12.5 kV; the polarity of the output voltage depends upon the HV power supply setting (Section III-G).

Typical pulses for the TTL, deflector plate voltages, and the "on" or "off" states of the MOSFET stacks are shown in Fig. 8. The top waveform of Fig. 8 shows an example of a TTL pulse sequence. The next waveform shows the corresponding output voltage for Plates "A". Plates "A" in Fig. 8 refers to either both of the top plates or to both of the bottom plates of the two pairs of deflector plates. The next two waveforms show the "on" or "off" state for the pull up and pull down stacks, respectively, that drive Plates "A".

The next waveform shows the output voltage for Plates "B". Plates "B" in Fig. 8, refers to either both of the bottom plates or to both of the top plates of the two pairs of deflector plates. The two next waveforms show the "on" or "off" state for the pull up and pull down stacks, respectively, that drive Plates "B".

The relative switching time of each of the MOSFETs in a stack is critical to minimizing the losses in a MOSFET (Section IV). The fiber optic receivers are the most significant contributor to differences in relative timings. The relative timing of the turn-on of the MOSFETs on each card is trimmed (Section IV). However, this does not compensate for pulsewidth distortion (PWD). Total PWDs in the range of 5–15 ns have been measured for the combination of fiber optics, DEIC420A MOSFET drivers, and DE375-102N12A MOSFETs. The controls exhibit a minimum propagation delay of approximately 12 ns from receipt of a TTL signal to driving the HFBR-1528 transmitters to turn on or off a stack. A programmable delay line allows for the turn-on drive to the HFBR-1528 transmitters to be delayed relative to the turn-off ($T_{\rm un}$ in Fig. 8). This allows the effect of PWD in the receivers to be compensated for so that there is no overlap between the conduction of the pull up and pull down stacks. For example, when the pull up stack is required to charge deflector plates "A" from 0 V to $+12.5$ kV:

1) The pull down stack has been on; the command to turn-off the pull down stack is issued by the controls. Neglecting the 12-ns propagation delay through the controls, the turn-off command is sent out coherently with the rising edge of the TTL pulse (Fig. 8).
2) There is a delay time of $T_{\rm un}$ during which both stacks are in the off-state (Fig. 8). As result of the relatively long time constant associated with charging the deflector plates ($\sim$1.5 ms), when both stacks are in the off-state, there is negligible change in the deflector plate voltage during delay $T_{\rm un}$. Hence, the voltage across the stack that has just turned off will remain at approximately 0 V.
3) At the end of delay time $T_{\rm un}$ the pull up stacks are turned on (Fig. 8). One stack turning on supplies current to charge:
   - one of the deflector plates "A";
   - the capacitance of the pull down stack which turned off time $T_{\rm un}$ earlier (Section III-E);
   - the capacitance to ground of the stack that is turning on (Section III-E).

Fig. 9 shows a controls card for the MuLan kicker; there is one such card in each modulator cabinet. Thirty-eight fiber optic transmitters are visible around the sides of the controls card. The

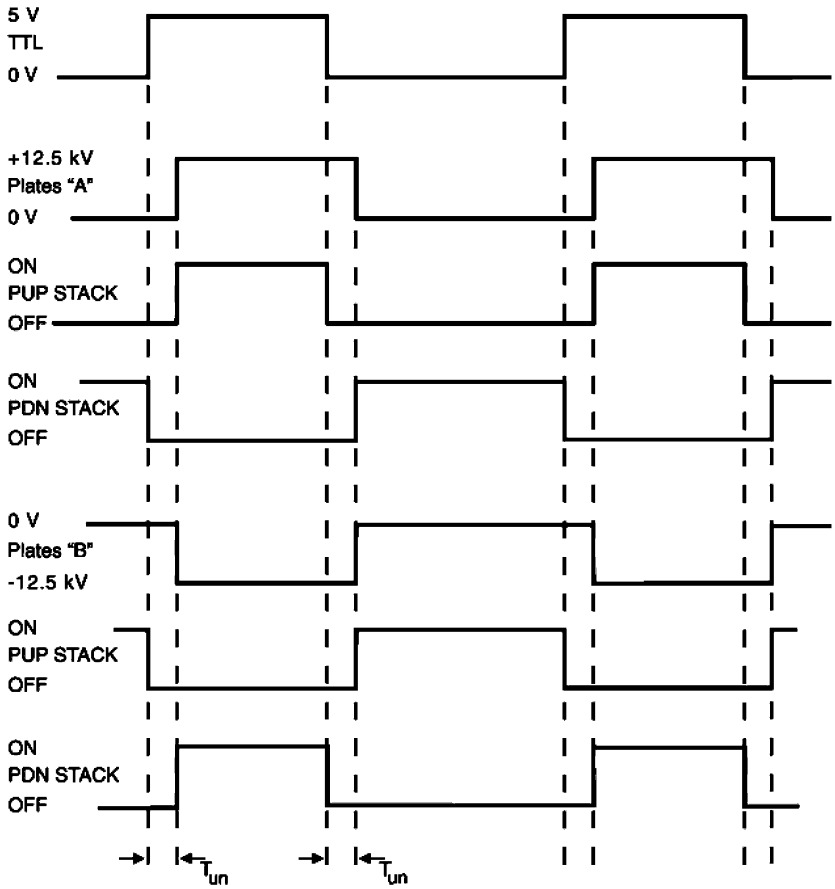


Fig. 8. Pulse sequences for MuLan kicker (neglecting propagation delay of 12 ns through controls card).

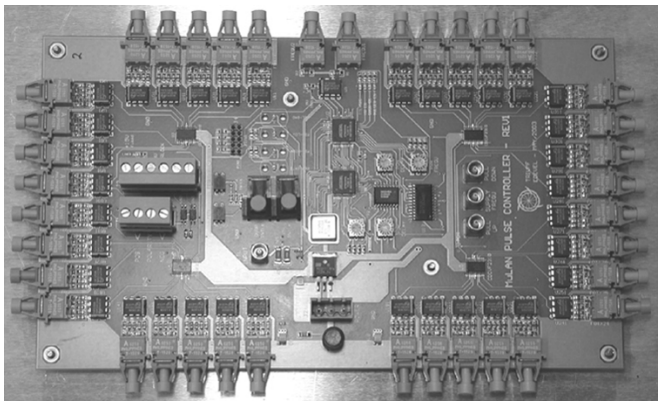

Fig. 9. Controls card for MuLan kicker.

two fiber optic transmitters in the center of the topside of the card provide the 90-kHz 1-$\mu$s command pulse for the primary side driver modules (see Section III-H). The other 36 fiber optic transmitters are arranged into two groups of 18. The 18 transmitters include one spare; 17 of each group of 18 transmitters provide the command pulses to each of the 1-kV modules in a stack.

The controls impose a minimum pulsewidth of 160 ns on the switching of the 1-kV modules in a stack; this is required for the following two reasons.

- In the event that a MOSFET turns off when it is still carrying considerable D-S current for charging the deflector plate capacitance, the current would be forced toward 0 A very rapidly (several nanoseconds). The energy stored in the magnetic field of the conductors could cause a high transient voltage across the D-S of the MOSFETs and they could avalanche, considerably increasing power dissipation in the MOSFETs if this occurs continuously.
- To prevent noise, generated by the high-voltage pulses, causing turn-off of the MOSFET drivers and MOSFETs while charging current is still flowing D-S (see previous item), and also to prevent retriggering of the 1-kV cards in a stack.

The on and off structure of the output command from the controls, to the 1-kV modules in each stack, is dependent upon the output polarity of the HV pulses. For example to produce a positive going HV output pulse (Plates "A" in Fig. 8) the pull down stack is turned off, and time $T_{\rm un}$ later the pull up stack is turned on. Similarly, to produce a negative going HV output pulse (Plates "B" in Fig. 8) the pull up stack is turned off, and time $T_{\rm un}$ later the pull down stack is turned on. Therefore, each control card has an input informing the controls of the polarity of the HV dc power supply. This input is only read during start-up of the 350-V power supply, to prevent noise from the HV output pulses causing the controls to inadvertently change the command sequence to the MOSFET stacks.

A 74F5300N fiber optic LED driver, from Philips [27], is used to drive each HFBR-1528 fiber optic transmitter The 745300N has a short propagation delay (2.5 ns), fast rise time (2 ns), and

high current drive capability (160 mA). An external pre-bias and pre-charging circuit is used for each transmitter. A low input to the 74F5300N driver results in no light out from the HFBR-1528 transmitter; no light into the HFBR-2528 receiver results in a high output from the receiver, which turns on the DEIC420A driver and DE375-102N12A MOSFET. Similarly, a high input to the 74F5300N results in the MOSFET being in the off state. Hence, the MOSFET turn-on is initiated by a falling edge into the 74F5300N driver.

## IV. Timing Considerations

The 1-kV modules (Fig. 2), containing the DEI MOSFET, have been shown to collapse 1000 V in less than 3 ns. This rapid collapse of voltage, combined with the maximum frequency of operation, if the MOSFETs in each stack do not turn on simultaneously, can result in significant dissipation in some MOSFETs. PSpice has been used to assess the effect of one MOSFET in a stack turning on late relative to all 16 other MOSFETs. The simulations show that, for a distributed inductance of 75 nH per module, a delay of 2 ns (4 ns) results in an additional dissipation of 7.1 W (17.9 W) above the nominal dissipation of 8.8 W, for 75-kHz operation at 12.5 kV. Therefore, it is important that the propagation delay for the turn-on command is well matched for all the modules in a stack. If the distributed inductance were increased to 150 nH per module a delay of 2 ns (4 ns) results in an additional dissipation of 1 W (6.2 W) above the nominal dissipation of 8.1 W, for 75-kHz operation at 12.5 kV.

The propagation delays through the HFBR-1528 fiber optic transmitters and HFBR-2528 receivers have been measured to be in the range of 98–111 ns. The propagation delays have been measured through two manufactured batches of the DEIC420A drivers and no correlation was found between batch number and delay. To allow spare modules to be used in any position, in the eight stacks, care has been taken to ensure that every 1-kV module has a similar propagation delay for the turn-on command edge ($158.3$ ns $\pm$ $0.4$ ns for the fiber optic receiver, DEIC420A driver, and DEI MOSFET, measured using a "reference" transmitter). This was achieved by initially matching DEIC420A drivers that had short propagation delays to a receiver with a long propagation delay and *vice versa*. In addition, the delay was trimmed via an *R-C* between the output of the receiver and the input to the DEIC420A (Fig. 2). The resistor R2 is nominally 680 $\Omega$; capacitor C11 is chosen to coarse tune the propagation delay and resistor RtrimT is used for fine tuning (Fig. 2). However, although this method permits the propagation delay of the turn-on command edge to be matched through the fiber optics, MOSFET driver, and MOSFET, there can be a significant PWD. To compensate for the PWD, a programmable delay line in the controls allows for the turn-on drive to the HFBR-1528 transmitters to be delayed relative to the turn-off (Section III-I).

## V. Measurements and Predictions

### A. TRIUMF

Without HV connected D-S, several 1-kV modules have been operated at 1.5 MHz continuous to demonstrate that they are inherently capable of high switching frequencies. Three prototype modules have been operated with a D-S voltage of 830 V per module and switching frequencies of 200 kHz, for several days continuously. Similarly, two series modules have been operated at 800-V D-S each and 500 kHz for three weeks continuously. No problems were encountered during these tests.

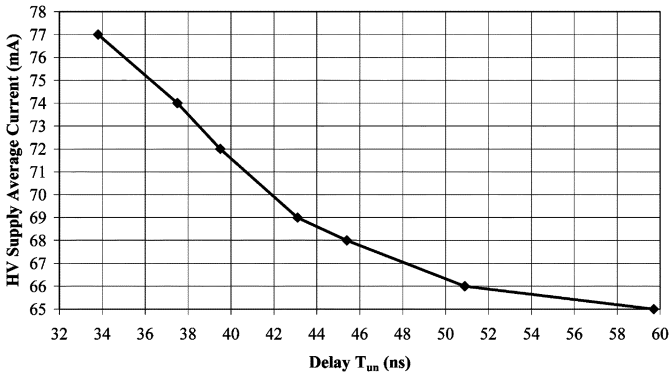


Fig. 10. Measured average current from HV power supply versus delay $T_{\rm un}$ for a single modulator operating at 6.25 kV and 75 kHz with an 80-pF load (meter resolution is 1 mA).

One MuLan modulator at a time was tested at TRIUMF, at frequencies of less than 0.01 Hz up to 77 kHz, with an 80-pF load, and output voltages of up to $\pm$12.5 kV. The 80-pF load consisted of a 77-pF HV coaxial cable and 3-pF parasitic capacitance of a Tektronix P6015A 1000:1 HV probe [28]. The 77-pF coaxial cable load was chosen as its value closely approximates the expected output load (74 pF) of the deflector plates, supports and connections (Section I).

The average current drawn from the HV power supply, when operating at 6.25 kV and 75 kHz with an 80-pF load, was predicted to be 60 mA. However, when a modulator was initially operated, with a delay $T_{\rm un}$ of 34 ns (Fig. 8), the average current was 78 mA. The average current was measured as a function of delay $T_{\rm un}$ (Fig. 10). The maximum delay of $T_{\rm un}$ is 60 ns; the average current with this delay is 65 mA. With $T_{\rm un} = 60$ ns, the measured average current is 8% greater than expected.

There is little further reduction in average current as the delay is increased beyond 51 ns (Fig. 10), and the increased delay would have the undesirable effect of increasing the total propagation delay through the modulator. Therefore, $T_{\rm un} = 51$ ns was chosen as the operating point for the modulators.

The average current drawn from the HV power supply, when operating at 12.5 kV, with an 80-pF load, was measured at 40 kHz with $T_{\rm un} = 34$ ns and $T_{\rm un} = 51$ ns. This average current is 20% greater at $T_{\rm un} = 34$ ns compared to $T_{\rm un} = 51$ ns; this is consistent with the results of measurements at 6.25 kV (Fig. 10).

Rise and fall times (10%–90%) were measured using the P6015A HV probe. The 10%–90% rise and fall times of a 12.5-kV 70-kHz output voltage pulse have been measured to be 40 and 39 ns, respectively, with an 80-pF output load. The corresponding rise and fall times predicted by PSpice are 41 ns.

An average current of 100.3 mA was predicted using PSpice for operation at 12.5 kV and 65 kHz, with the 80-pF output load. The corresponding measured average current is 100 mA, with a delay $T_{\rm un}$ of 51 ns; the meter resolution is 1 mA. The measured average current corresponds to 1.54 mA/kHz at 12.5 kV. The

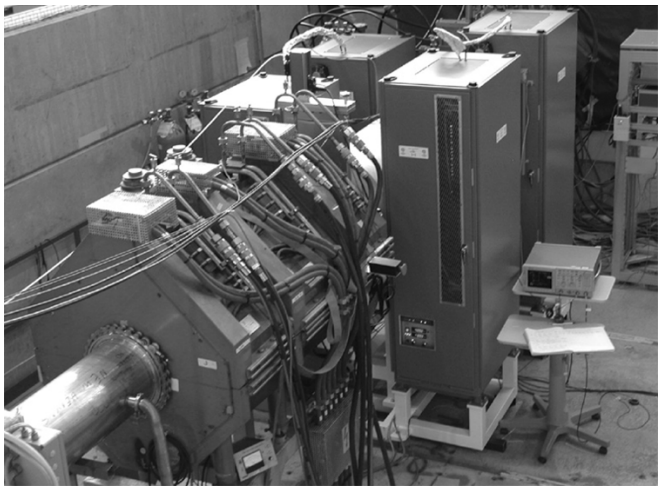

Fig. 11. Four modulators of MuLan kicker installed in beam line at PSI.

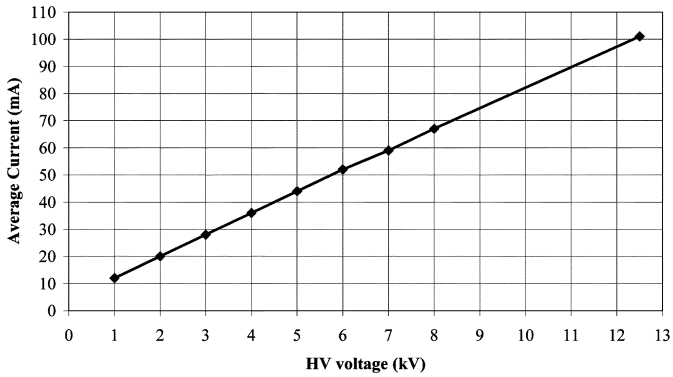


Fig. 12. Measured average current from HV power supply versus HV setting, for two modulators driving a single pair of deflector plates, operating at 65 kHz (meter resolution is 1 mA).

excellent agreement between measured and predicted average current indicates the following.

- Total effective capacitance of the MOSFET stacks and output load is close to the simulated value. This is also consistent with the measured rise and fall times being close to the predicted values.
- Cross conduction between a pull up and pull down stack with $T_{\rm un} = 51$ ns is small; from Fig. 10, remaining cross conduction is estimated to result in an increase in average current between 1.5% and 3%.

### *B. PSI*

Subsequently, the four modulators were installed in the beam line at PSI (Fig. 11), commissioned and operated successfully at $\pm$12.5 kV. Detailed measurements were carried out on the kicker system at PSI. The average current drawn from each of the two HV power supplies, with the kicker driving one set of deflector plates, at 64.1 kHz and $\pm$12.5 kV was 100 mA (the meter resolution is 1 mA), i.e., 1.56 mA/kHz. This is very close to the 1.54 mA/kHz measured for a single modulator driving an 80-pF load at TRIUMF (Section V-A). This good correlation indicates that the effective parasitic capacitance of the deflector plates, support structure, feed-throughs, and connections is close to 80 pF.

The modulators were operated over a frequency range from 9 to 65 kHz to confirm that the average current drawn from the HV power supply at a given voltage setting is directly proportional to the output frequency of the modulators.

One pair of deflector plates was driven with a voltage pulse magnitude in the range 1–12.5 kV, at a frequency of 65 kHz. The average currents drawn during these measurements are shown in Fig. 12; from 1 to 6 kV the slope of the line is 8 mA/kV; between 6 and 12.5 kV the slope is 7.6 mA/kV.

One modulator was operated driving one of the deflector plates at 12.5 kV and the other plate of this set of plates was held at ground. The average current drawn from the HV supply corresponded to 1.43 mA/kHz. The 8.3% reduction from 1.56 mA/kHz, when both of a pair of deflector plates are driven, is attributable to the absence of the virtual ground halfway between the plates when only one plate is driven. The 8.3% reduction in current is consistent with a reduction in effective load capacitance of 10.4 pF. A reduction in effective capacitance of the deflector plates by 9.8 pF was expected from 3-D simulations (Section I).

TABLE II
MULAN KICKER SPECIFICATIONS AND MEASUREMENTS

| Parameter | Specification | Measured |
|---|---|---|
| Maximum propagation delay ($T_{un}$ = 34 ns) | 200 ns | 200 ns |
| Minimum pulse width | 200 ns | 160 ns |
| Rise/fall time | 45 ns | 40ns/39ns |
| Max. repetition rate | 50 kHz | 77 kHz |
| Output voltage | ±12.5 kV | ±12.5 kV |

The kickers produced RF noise at a level greater than is acceptable for the sensitive detector required for the MuLan experiment. Measurements confirmed that the sources of the RF noise are due to both grounding and RF radiation. The RF noise was measured using a 1-m-long antenna situated a distance of 5 m from the cabinets. Fourier analysis of the RF noise showed that it consisted mainly of 8- and 35-MHz components. Rearranging some of the grounding significantly reduced the RF noise. However, the peak of the RF noise, in the time domain, is still approximately 12 V for operation at $\pm$12.5 kV. Further work is required to reduce the peak to an acceptable level of approximately 0.1 V.

## VI. CONCLUSIONS AND ONGOING RESEARCH

One of the $\pm$12.5 kV modulators has been tested at TRIUMF and meets or exceeds the requirements, as shown in Table II.

The four modulators were installed in the beam line at PSI at the end of July 2003 and meet the specifications of output voltage, maximum repetition rate, rise and fall times, and minimum pulsewidth.

There are some RF noise problems, with the system at PSI, that are currently being investigated. These problems are thought to be attributable to ground currents as well as RF radiation.

A similar kicker system is required for an experiment at TRIUMF [29]. Further development work is planned, especially in the area of the fiber optics, which proved to be very time consuming to trim their delays. In addition, there may be

long-term issues associated with drift of the relative timing of the fiber optic transmitters and receivers.

There is a requirement for a radio-frequency quadrupole (RFQ) at TRIUMF, which is required to produce voltage pulses at a rate of 3 MHz continuous. Resistor R10 (Fig. 2), which is 4.7 Ω and 0.25 W in the MuLan kicker design, has been replaced by a 1.2-Ω 1-W resistor to allow for operation at frequencies up to 5 MHz. Similarly, for the RFQ, the flat heat sink used for the MuLan kicker has been replaced with a larger heat sink with fins. Two 1-kV cards have been operated in push-pull at 3.5-MHz and 500-V drain-source, driving a capacitive load of 105 pF [30]. In order to provide the energy for the on-board 16-V dc power, the 1-$\mu$s–wide pulses, through the primary winding of the two cards, was operated at 340 kHz. The primary current pulses were obtained from a heavily filtered 60-V power supply in series with an 8-Ω power resistor.

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