

Kicker status, March 23, 2005

Françoise Mulhauser,
University of Illinois at Urbana-Champaign, USA

July 30, 2006

1 Introduction

During my visit at TRIUMF, Mike showed me the situation with the kicker. He spend a good amount of time explaining what Gary and him were doing to improve the kicker performance and avoid “killing” discharges.

Two adaptations were made on the kicker.

- Two parallel $6.2\ \Omega$ resistors were added on each MOSFET card, to give a total of $3.1\ \Omega$. This will allows the system to react less to the presence of a big current.
- A current interlock system with a $0.25\ \Omega$ resistor and LED signal is installed on each MOSFET series (two per cabinet) to forbid the cards to turn-off if an over-current is present.

Some pictures were taken, showing the actual test system at TRIUMF (see Figs. 1– 3). Only one MOSFET card can be tested at each time.

While I was present, Mike did some measurements with various configurations.

- Card without (car # 187) and with (card # 37) the additional resistors.
- Interlock system active and inactive.
- Various pulse widths.

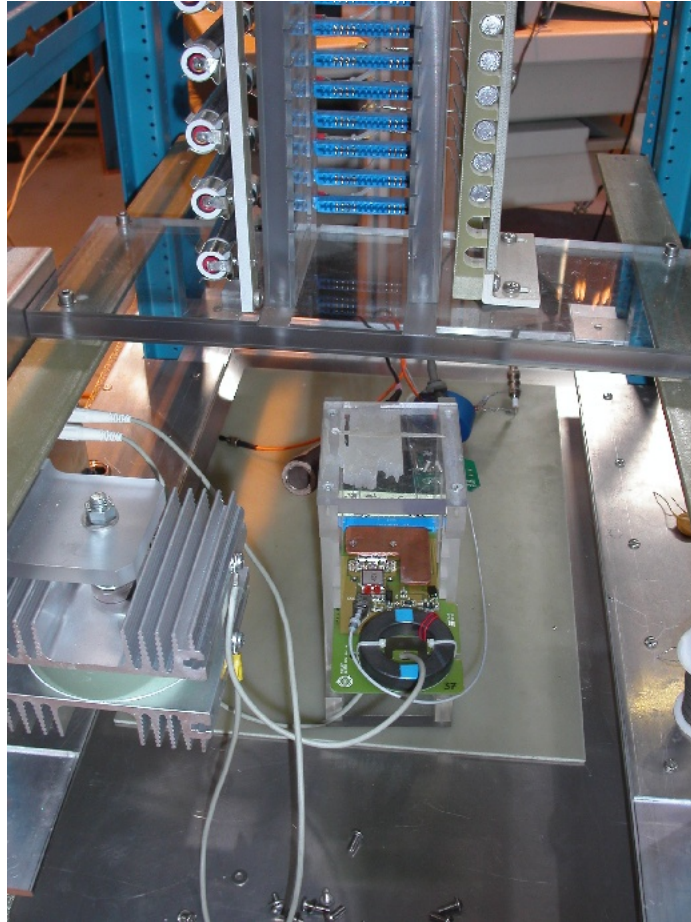


Figure 1: *One MOSFET card installed in the test system.*

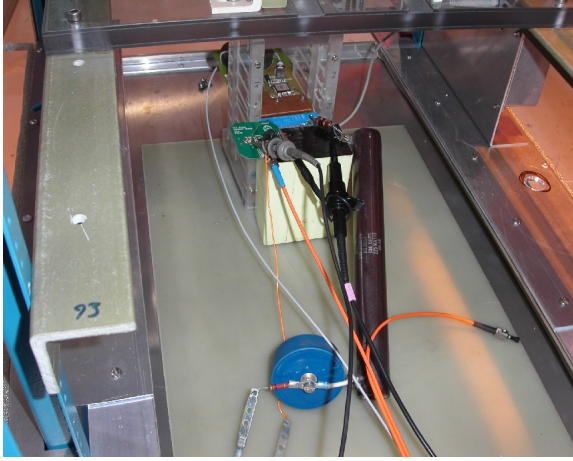


Figure 2: Additional resistor (small in the back of the photo) and capacitor to fake over-current. (Note, the big resistor is just for limiting current from DC power supply and does not take pulse current).

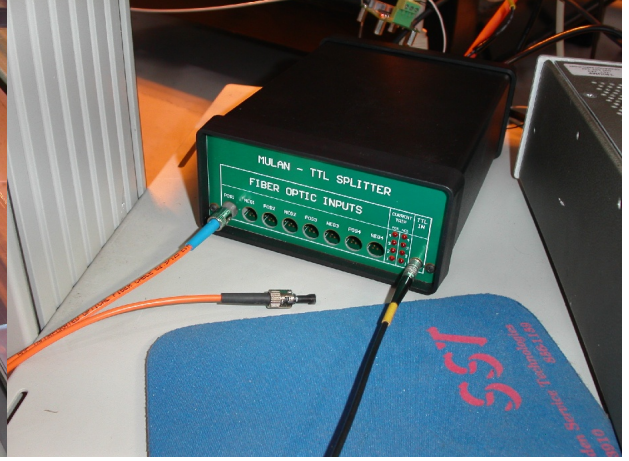


Figure 3: External box of the current interlock system and the TTL splitter.

2 Measurements

Results are all given in Figs. 4– 12. For each figure, one sees four signals.

1. The green signal is an inverted TTL pulse width (control card is not present) send to the kicker, as our MB would do.
2. The blue signal is the fault monitor. It exists only when the current interlock system is installed. A high signal is a fault value.
3. The brown signal is the drain–source voltage, measured directly on the MOSFET.
4. The purple signal is measured across the $0.25\ \Omega$ resistor in the interlock system. When its value is lower than 1.7 V, which correspond around 8 A, the fault blue signal is stopped.

2.1 Inactive Interlock system

The effect of the additional gate resistors is a decrease of the drain–source collection. One can see this effect by comparing Figs. 4 and 5. It is important to see the ringing has decreased a lot with the gate resistor. As can be seen, the brown signal is proportional to the over-current voltage which is send. However, the remaining brown signals, once the MOSFET has turned off, is reaching 450 V drain–source without gate resistor and only 250 V drain–source with gate resistor (note the vertical scale is 100 and 50 V, respectively). It is a fact that with the MuLan MOSFET card, the voltage could reach more than 450 V during this test. Card # 187 reaches only 450 V because of a relatively high inductance. Indeed, the wide gate trace has been cut ready for the additional two resistors, but then has been re-soldered with a single thin wire rather than the wide trace.

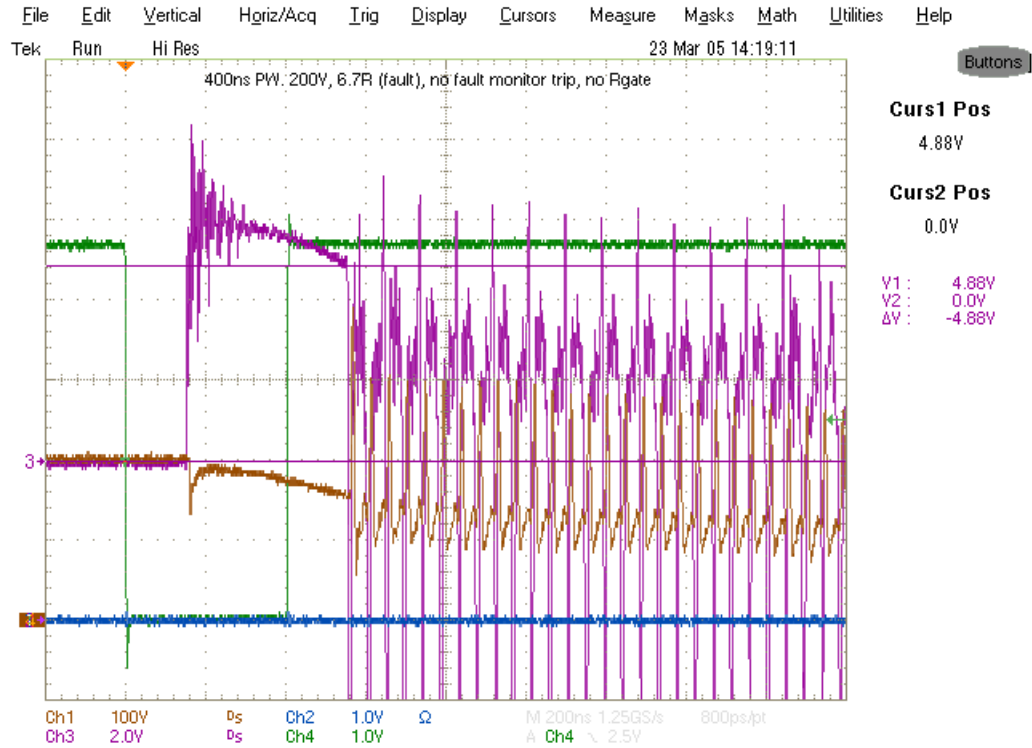


Figure 4: *Inactive interlock system without gate resistor. Over-current simulated with 200 V and kicker pulse width at 400 ns.*

We did not make any measurement without the resistors at higher over-current, to avoid damaging more MOSFET cards.

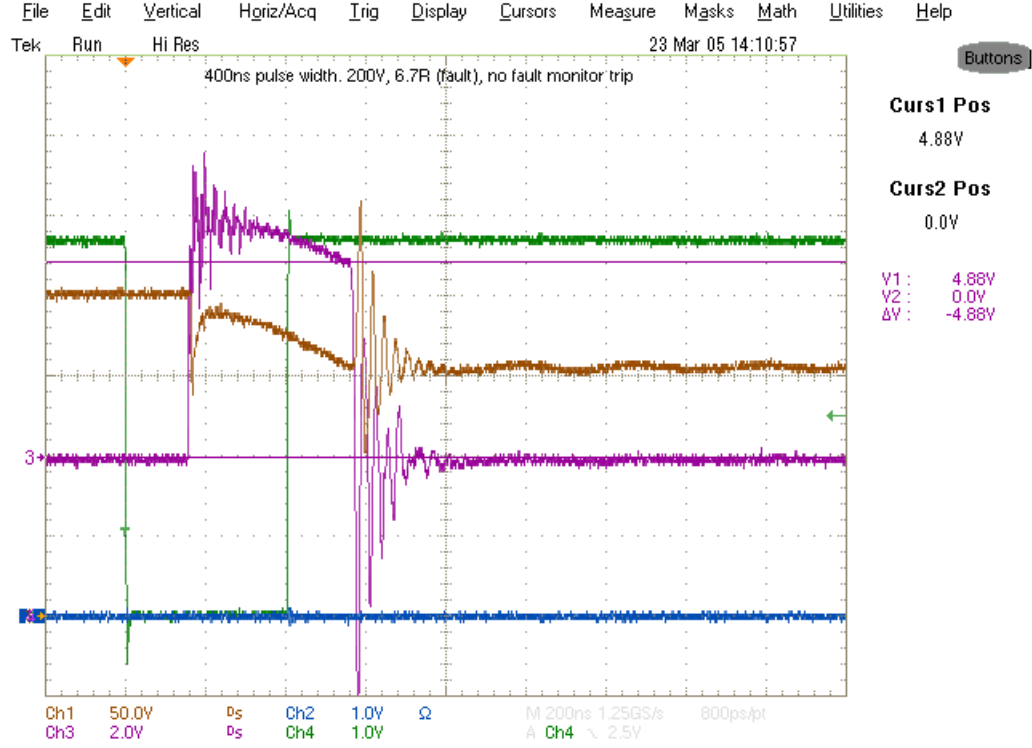


Figure 5: *Inactive interlock system with gate resistor. Over-current simulated with 200 V and kicker pulse width at 400 ns.*

With the installed gate resistors, we compare the effect of 200 V drain-source (Fig. 5) and 600 V drain-source (Fig. 6) on two parallel, 1 W, carbon resistors shown in Fig. 2. The measured voltage as seen via the purple signal moves from 4.9 V to 12.9 V, which is reaching a current of 52 A. If one decreases the pulse width from 400 to 200 ns (Fig. 7), one sees an additional increase in the voltage up to 14.2 V, which correspond to nearly 56 A. As you can imagine, the MOSFET were still working at the end of the test, which means that they are supporting such a big current, due to the presence of the gate resistor.

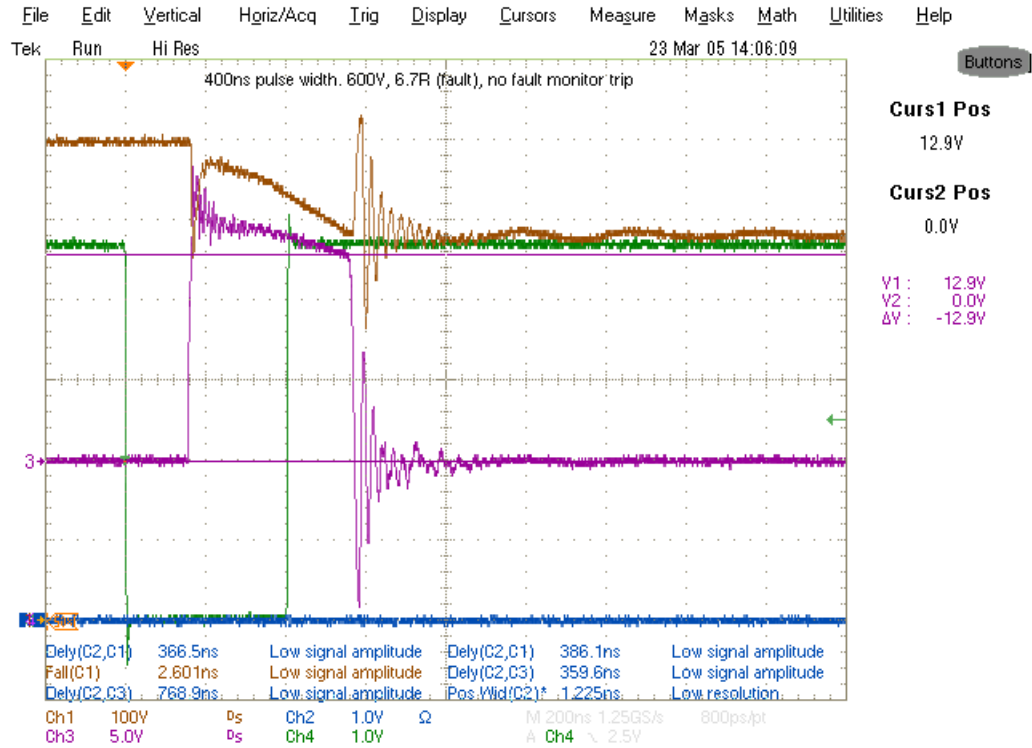


Figure 6: *Inactive interlock system with gate resistor. Over-current simulated with 600 V and kicker pulse width at 400 ns.*

The previous measurements are already showing the effect of the resistor and the question of the pulse width. We are now passing to measurements with the interlock system active.

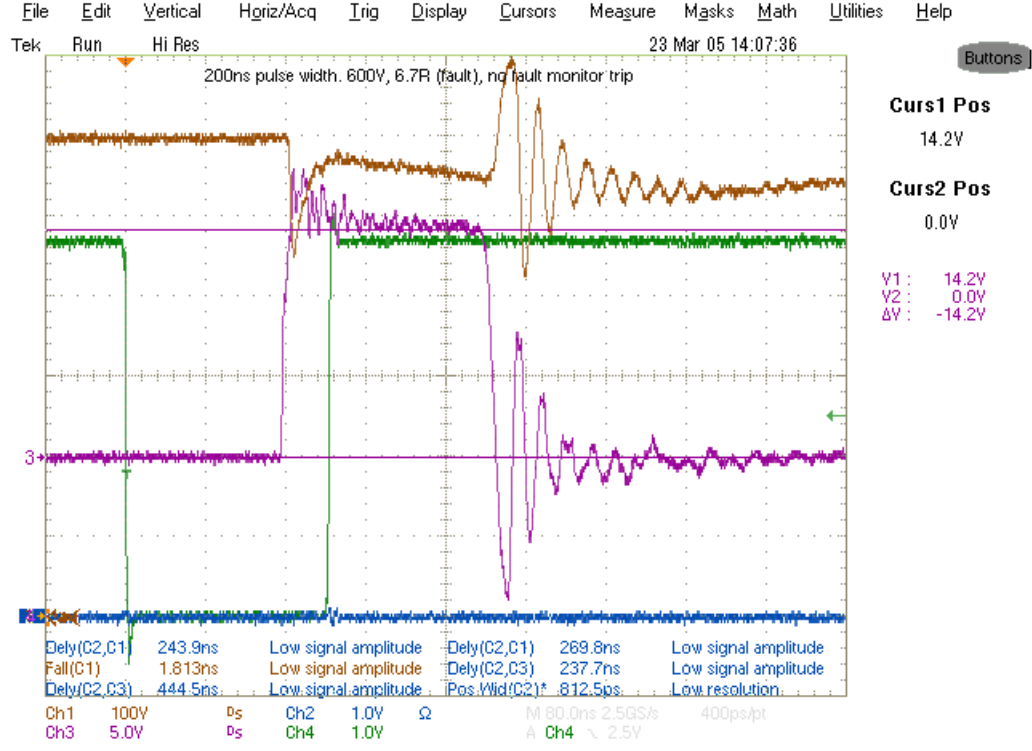


Figure 7: *Inactive interlock system with gate resistor. Over-current simulated with 600 V and kicker pulse width at 200 ns.*

2.2 Active Interlock System

Measurements are performed with the scope and the MOSFET on a single trigger mode to avoid repetitive case and damage on the card.

Figures 8– 10 are showing the effect of the interlock system on the MOSFET card without additional gate resistor. The level of the brown signal is proportional to the drain–source voltage. As can be seen, the green signal does not turn itself back off, because an over-current has been seen on the purple signal. The MOSFET card is staying in its on state. The blue signal width is proportional to the time, the purple signal is above the 1.72 V limit. Its width varies from 2 to 3.2 and 4 μ s.

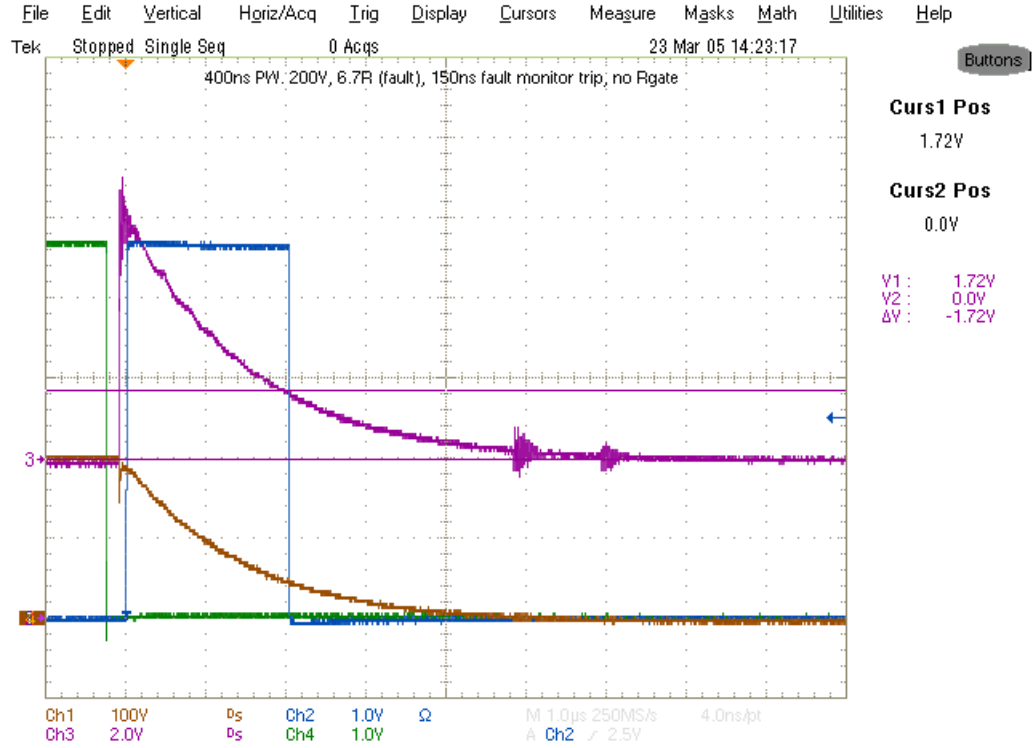


Figure 8: *Active interlock system without gate resistor. Over-current simulated with 200 V and kicker pulse width at 400 ns.*

Comparing now Fig. 10 (no gate resistor) with the addition of the gate resistor on the MOSFET card, Fig. 11, one can see that the source-drain collection is much lower with the resistor. We were measuring 600 V source-drain without gate resistor and we do measure only 400 V source-drain with the gate resistor. The rest of the scope traces are similar, because the interlock system has taken place and no more switch are occurring. Figure 11 correspond to what we expect to have during normal measurement time, if the interlock has to take place.

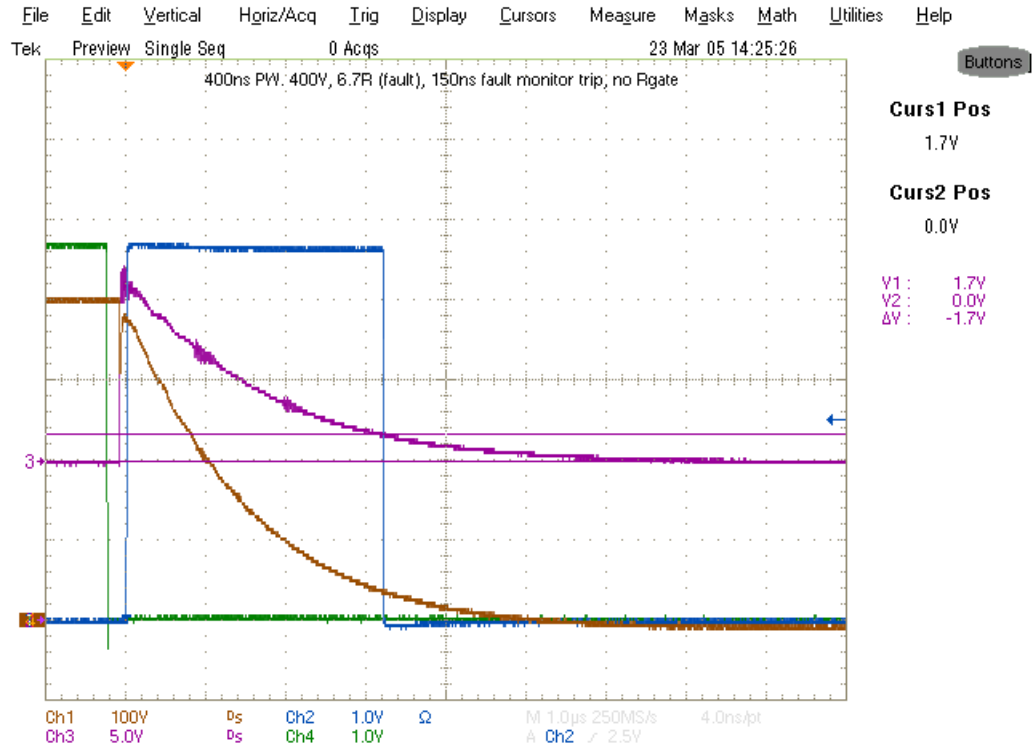


Figure 9: Active interlock system without gate resistor. Over-current simulated with 400 V and kicker pulse width at 400 ns.

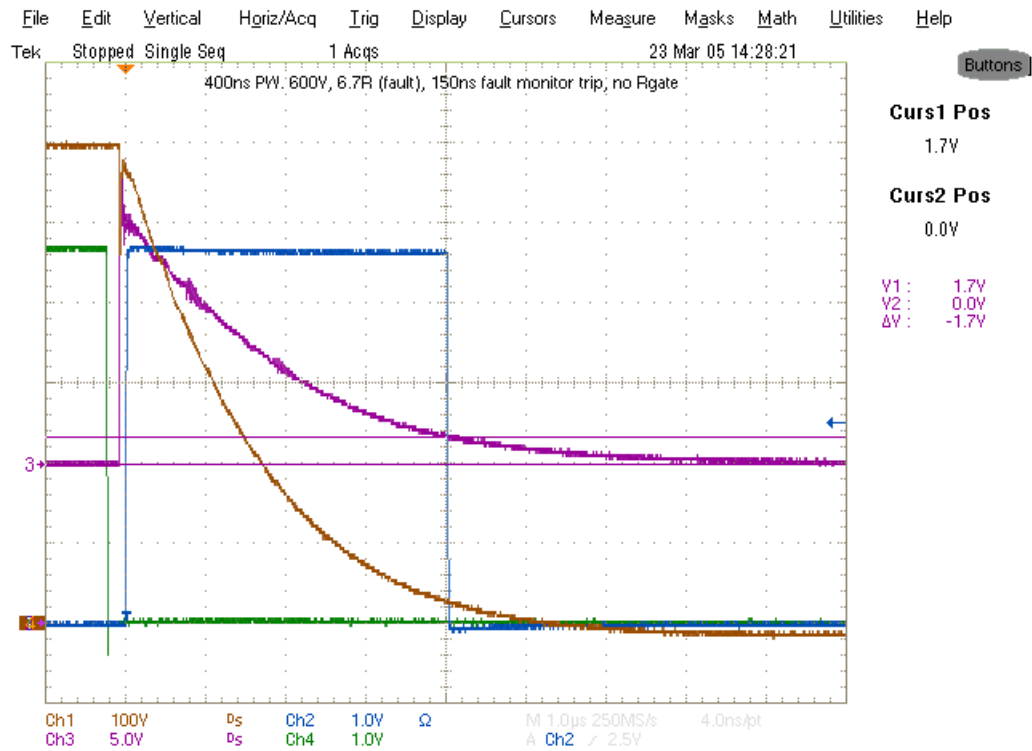


Figure 10: Active interlock system without gate resistor. Over-current simulated with 600 V and kicker pulse width at 400 ns.

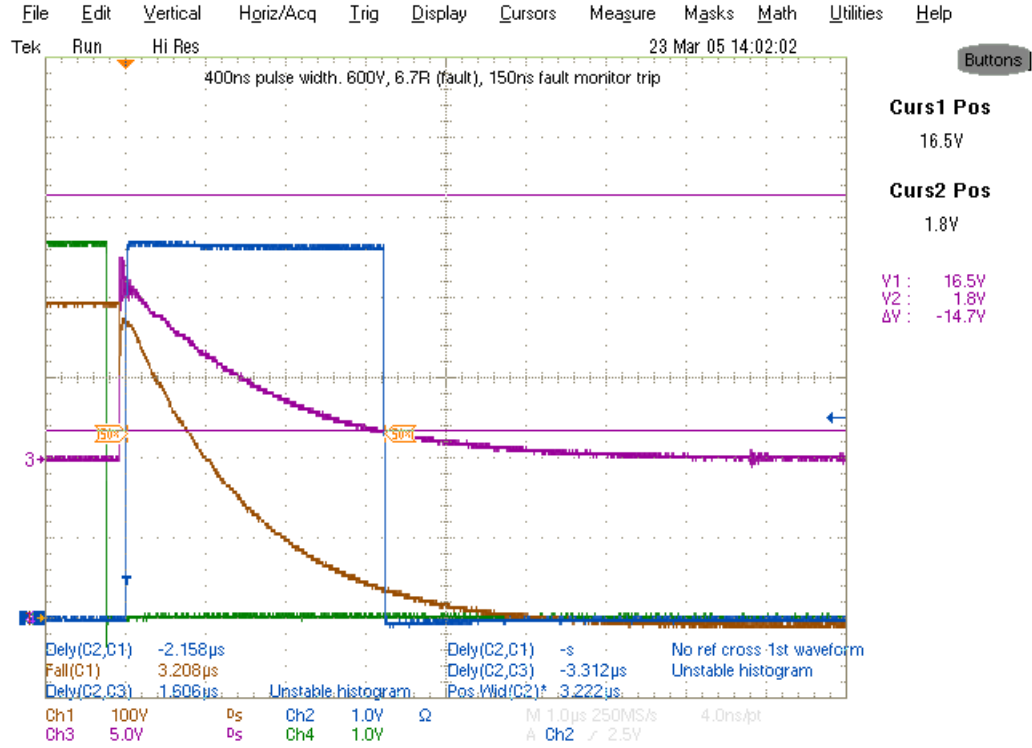


Figure 11: Active interlock system with gate resistor. Over-current simulated with 200 V and kicker pulse width at 400 ns.

A last measurement was done by decreasing the TTL pulse width from 400 to 200 ns, below a time necessary for all the interlock system to take place. Figure 12 shows what is then happening. The TTL signal switch the MOSFET off before the interlock has been able to react. Therefore, there is a burst of current in the source–drain signal, creating a potential hazard for the MOSFET card. This shows us that the TTL pulse width has to be bigger than internal delays of the system. A width of 400 ns is the minimal that we should use safely.

This document is a summary of my understanding of what will happened with the kicker once remounted at PSI. I hope that I am not misleading too much. Comments, corrections, and reactions are more than welcome.

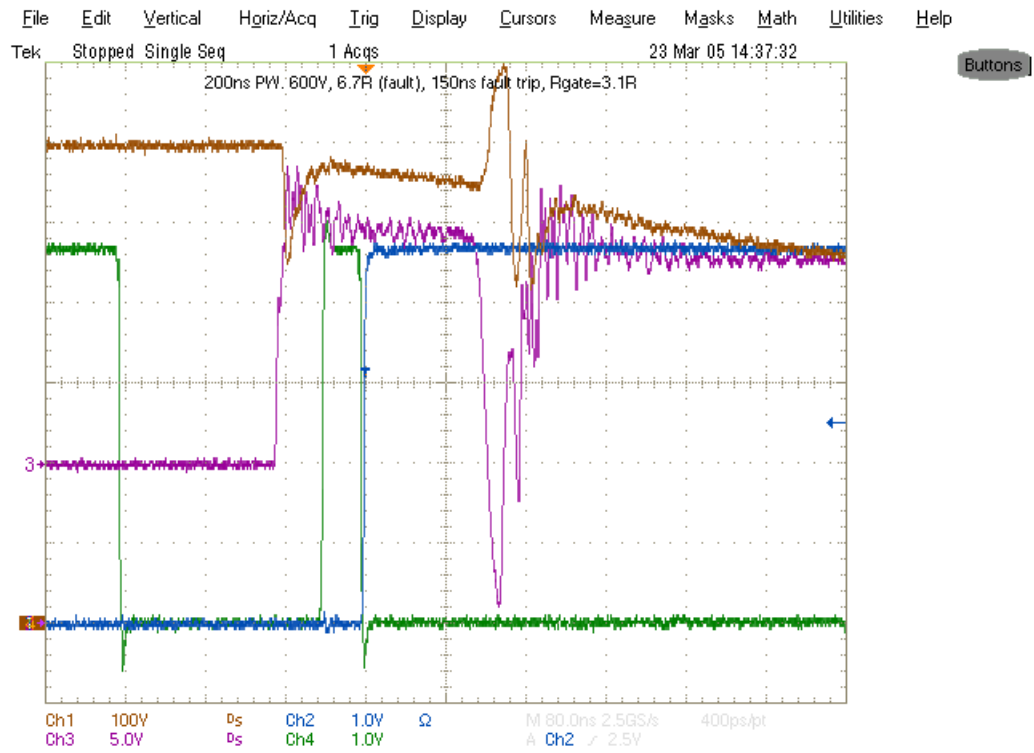


Figure 12: Active interlock system with gate resistor. Over-current simulated with 600 V and kicker pulse width at 200 ns.