The Digital Silicon Photomultiplier – System Architecture and Performance Evaluation

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***Abstract*–In this paper we present the first fully digital implementation of the Silicon Photomultiplier. The chip design is based on the technology demonstrator chip presented in [3]. The new sensor represents a self-contained detector including a JTAG controller for configuration and test, single-ended and differential clock and test input signals, an integrated acquisition controller and two serial data outputs.**

The sensor is based on a single photon avalanche photodiode (SPAD) technology integrated in a standard CMOS process flow. Photons are detected directly by sensing the voltage at the SPAD terminal using a dedicated cell electronics block next to each diode. This block also contains active quenching and recharge circuits as well as a one bit memory for the selective activation of individual detector cells. A balanced trigger network is used to propagate the trigger signal from all cells to the two integrated time-to-digital converters. Photons are detected and counted as digital signals, thus making the sensor less susceptible to temperature variations and electronic noise. The resulting data packets are transferred to the readout system through a serial data interface.

In this paper, we discuss the new sensor architecture and evaluate its performance.

I. Introduction

RECENTLY the Silicon Photomultiplier (SiPM) gained interest as a potential candidate to replace photomultiplier tubes for reasons of ruggedness, compactness and insensitivity to magnetic fields [1,2]. Other advantages of solid state detectors in general are their low operating voltage, low power consumption and large scale fabrication possibilities. Today, silicon photomultipliers operate in an analog way. The passively-quenched Geiger-mode cells of the SiPM are connected in parallel through a long interconnect, and the resulting output signal is therefore the analog sum of the individual currents of all cells. Hereby, the good intrinsic performance of the SPAD is not fully utilized, as the generated signal is deteriorated by the relatively large parasitics of the on-chip interconnect, the bond wires and the external load.

In [3,4] we presented the digital Silicon Photomultiplier technology demonstrator and showed how this new detector concept can overcome some of the deficiencies of the analog Silicon Photomultiplier. In this contribution, we will show further results of the new fully integrated digital Silicon Photomultiplier and discuss some aspects of the new sensor architecture.

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II. Sensor Architecture

The technology demonstrator chip described in [3] was designed as an experimental vehicle to develop and test the acquisition sequence and to evaluate the basic performance of the sensor for different applications. Therefore, a flexible architecture was chosen and the acquisition controller has been implemented in the controlling FPGA located on the test board. This flexibility, however, implied a large number of bond wires needed to control the sensor. Consequently, the next development step was to integrate the acquisition controller on the same chip. Additionally, test circuitry had to be added to facilitate fast in-line testing of the sensors.

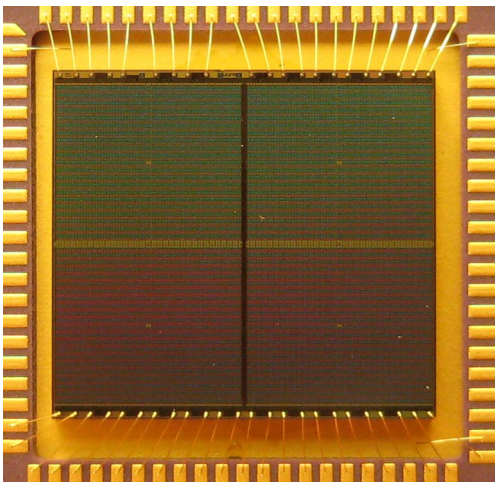

Fig. 1. The Digital Silicon Photomultiplier Prototype. The sensor consists of a 2x2 pixel arrangement. The chip size is 7.8x7.2mm² containing 25584 single photon avalanche photodiodes.

The new sensor shown in Fig. 1 consists of an array of 2x2 SiPM pixels with 6396 single-photon avalanche photodiodes each. The diodes are arranged in a 64x100 matrix with four diodes left out at the center of each pixel to create space for additional circuitry. The pixel design itself is to a large extent based on the design previously validated in the technology demonstrator chip DLD8K. Also, the peripheral circuits are similar to the previous design except that additional scan-test logic has been added for fast in-line testing. All four pixels are controlled by dedicated pixel controllers placed in the vertical gap between the pixels. Two time-to-digital converters with a modified design have been added and placed in the horizontal row between the pixels. The trigger levels of each pixel can be adjusted to 1, ≥2, ≥3 and ≥4 photons and the resulting pixel trigger signals are combined together to generate the master trigger signal for the main acquisition controller. The

controller provides the same control signals to all four pixels. This means that with respect to the trigger signal, the chip behaves as one SiPM pixel. Each acquisition results in four photon counts, one per pixel, and two correlated time stamps.

The new sensor chip is designed to operate on 200MHz reference clock, which can be supplied either via single-ended (LVCMOS) or differential (LVDS) inputs. Also, the electrical test input (SYNC) used to test and calibrate the TDCs can be supplied either in single-ended or differential configuration independent of selected clock configuration, to provide maximum flexibility for the system builder. When using differential inputs for clock and sync, the single-ended IO pads can be internally re-configured to provide additional external trigger input and internal trigger output. Using these signals, multiple sensors can be connected to trigger groups, so one sensor is capable to start acquisition in one or more of its neighbors.

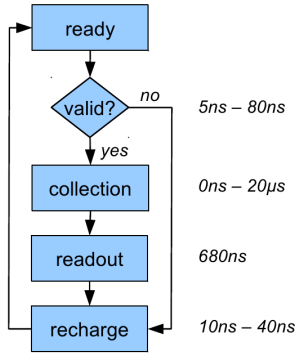

Fig. 2. The state diagram of the integrated main acquisition controller. Most of the timings can be programmed during chip configuration via the JTAG interface.

The acquired event data is transferred via two 100 MHz serial data links to the readout infrastructure. The transfer is independent of the acquisition and no additional dead time is introduced. Even for the minimum acquisition time, the sensor is capable of outputting data faster than acquiring new data. A typical acquisition sequence is shown in Fig. 2. The controller starts in the ready state waiting for the trigger signal. Some user-programmable time after the detection of the trigger signal, the controller continues with testing the event validation signal, which is used to separate real event triggers from dark count generated triggers. If a dark count trigger is detected, the controller changes to the recharge state for a user-specified time to reset all the diodes in the array. Subsequently, the controller state changes to ready state again. The minimum recovery time in case of a dark count trigger is 20ns. In case the event is validated, the controller state changes to the collection state, a programmable delay intended to detect the photons impinging on the sensor. The collection time can be adjusted up to 20µs. During the fixed readout time, the acquired photons are accumulated and written to the output buffers. The controller changes via the recharge state to ready state again, totaling a minimum acquisition time of 695ns. The timings of the individual phases of the acquisition sequence can be programmed using the JTAG interface, which is also used to program the cell inhibit memory. Using the JTAG interface for configuration has the advantage of being able to daisy-chain several sensors into a single JTAG chain, thereby simplifying the electrical interface to a sensor tile [5].

A. Time-to-Digital Converter

The integrated time-to-digital converters have a typical bin width of 24ps under nominal operating conditions. Fig. 3 shows the distribution of the bin width values for one particular sensor. Two time-to-digital converters running with complementary 100 MHz clock have been integrated to provide at least one valid time stamp for every event. To counteract the meta-stability close to the reference clock edge, the TDC design has been modified and a 500ps wide exclusion window has been added. As both TDCs are running 180° out of phase, both TDCs deliver a valid time stamp for 90% of all events, which can be used to further improve the timing accuracy.

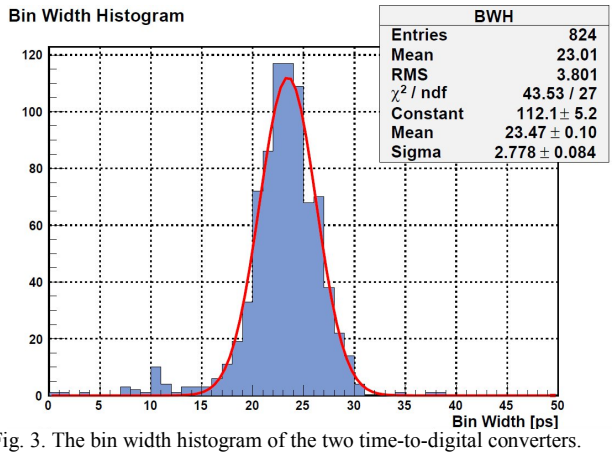

Fig. 3. The bin width histogram of the two time-to-digital converters.

The cross-correlation between the time stamps of the two TDCs is shown in Fig. 4. This two-dimensional histogram is generated by using the time stamps of random events. The histogram can be used to generate the look-up table used to correct for the TDC non-linearity.

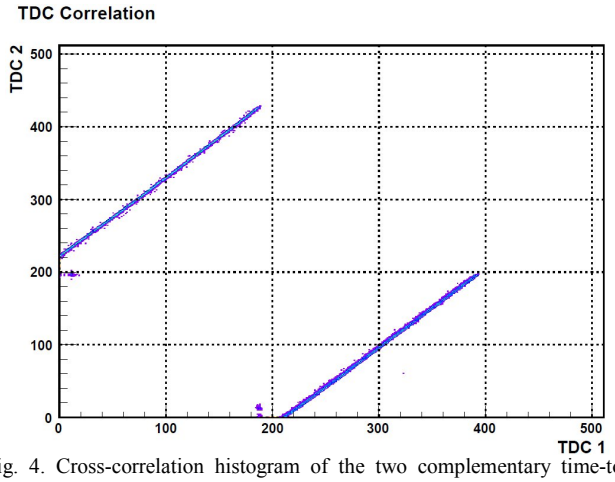

Fig. 4. Cross-correlation histogram of the two complementary time-to-digital converter time stamps for randomly generated events.

The non-linearity of the two time-to-digital converters for a particular sensor is shown in the following Fig. 5. The non-

linearity represents the fabrication-related deviations from the average bin width over the length of the TDC. This non-linearity can be completely corrected by the FPGA look-up table.

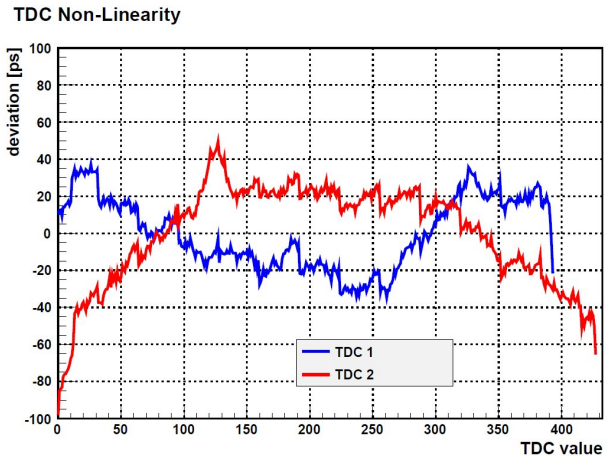

Fig. 5. The deviation from the ideal TDC response for a randomly chosen sensor.

B. *Trigger Network*

The aim of the trigger network is to provide a low-skew signal path from each micro-cell to the time-to-digital converters. It also provides some configuration options meant to increase the trigger threshold to higher photon levels to minimize system dead-time due to dark count related triggers.

The basic function of the trigger network has been explained in [3] with the comment that the trigger thresholds except for the first photon are statistical thresholds. This behavior is now shown in the following figure 6. The graphs show the individual probability of the n-th photon to generate the trigger, based on an analytical model of the trigger network.

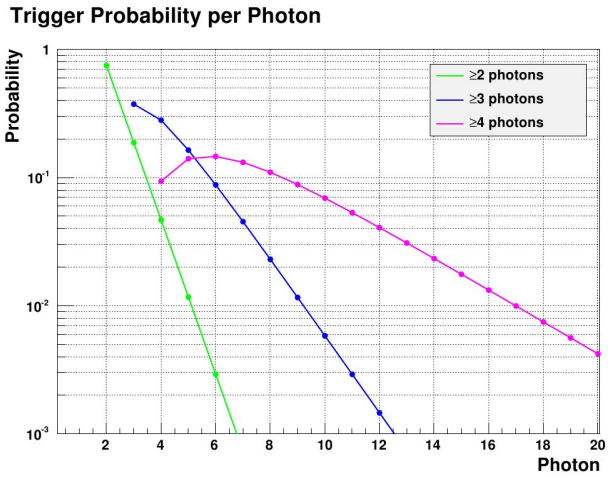

Fig. 6. The trigger generation probability for the n-th photon as a function of the selected trigger level.

As shown in the previous figure, for the ≥4 photon trigger network configuration, the 6th photon has the highest individual probability to generate the actual trigger signal. The actual trigger probability, as shown in Fig. 7, is given by the sum of the individual probabilities over the number of detected photons.

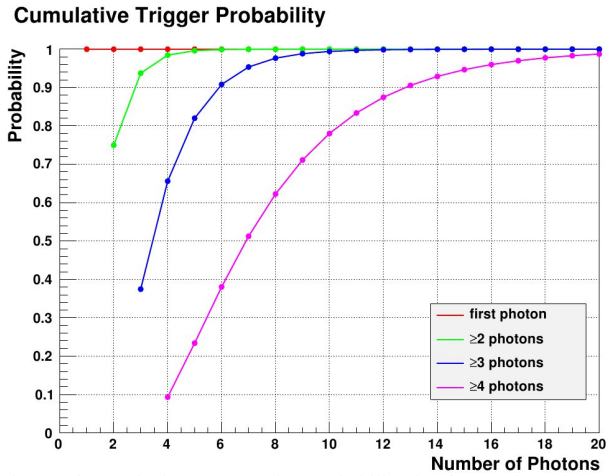

Fig. 7. The total trigger generation probability for the number of detected photons as a function of the selected trigger level.

Fig. 7 indicates that for the ≥4 photon trigger configuration, at least 7 photons have to be detected to reach 50% trigger probability level.

The validation logic is based on the same principle. The only difference is the number of regions the pixel is partitioned to, namely 32 in the current sensor configuration. This, together with the variable validation interval, allows one to set a higher energy threshold to discriminate real events from dark count events to reduce the system dead-time.

As mentioned previously, the trigger network has to provide a low-skew signal path from each cell to the TDC. This skew can be measured by measuring the signal propagation time for each cell separately and then subtracting the mean of the resulting distribution. The propagation time measurement is implemented using a picosecond-pulsed laser synchronized to the reference frequency. The resulting skew map is shown in Fig. 8.

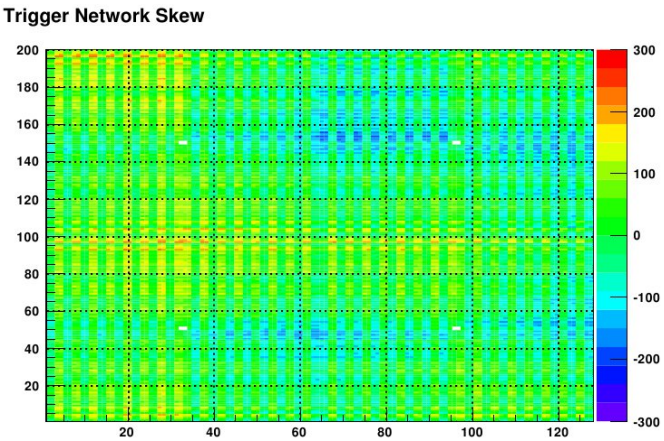

Fig. 8. The trigger network skew measured using a picosecond-pulsed laser source. The z-scale represents the skew in picoseconds.

The skew map of the sensor shows irregularities which can be linked to design structures. The measurement results will

be used as input for a sensor re-design, as the skew affects the sensor performance at single-photon levels. This is demonstrated in the next Fig. 9, showing the coincidence resolving time for two sensors in coincidence triggered by an attenuated picosecond-pulsed laser beam. The beam intensity has been varied to determine the time-resolution dependence.

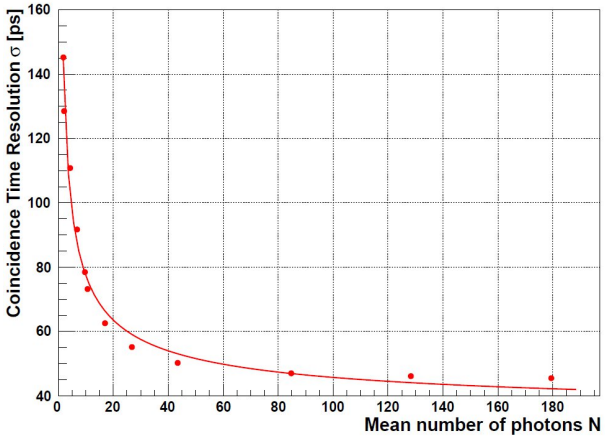

Fig. 9. Time resolution of two sensors in coincidence measured using a picosecond-pulsed laser source for different laser beam intensities.

III. Crystal Identification

A. Large Crystal Identification

One of the main tasks of the sensor is to identify the crystal that generated the light pulse. This is relatively easy to implement for large crystals one-to-one coupled to sensor pixels, as in most cases the detector pixel with the highest photon count can be used to identify the crystal. When using centroid computation, the floodmap in Fig. 10 clearly shows the four crystals and the Compton-scatter generated cross-connections between the crystals when illuminated by a ^{22}Na source. The energy resolution of this crystal arrangement was found to be 11% for all four crystals combined.

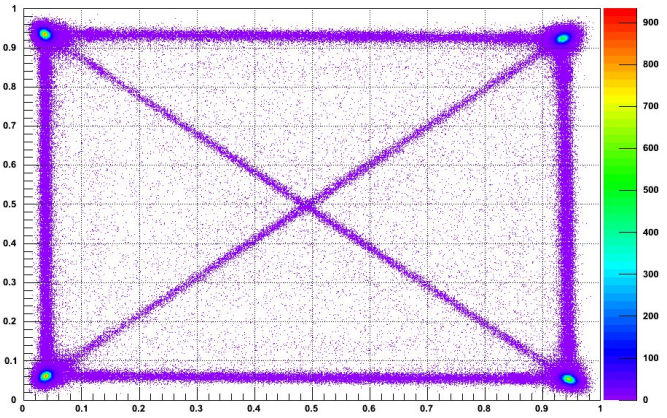

Fig. 10. Floodmap of an 2x2 array of 3x3x15mm³ crystals coupled one-to-one to the sensor and illuminated by a ^{22}Na source.

Event data was corrected for non-linearity due to sensor saturation, no other corrections were applied. The data was acquired in singles mode.

B. Small Crystal Identification

However, for small crystal arrays, the positioning strongly depends on the photon detection efficiency of the sensor. To estimate the efficiency of the sensor to resolve small crystal arrays, the setup was mounted on a precision XY stage and illuminated by a divergent picosecond-pulsed laser beam. The XY stage was stepped with 500µm steps in both directions and the resulting data has been analyzed and the floodmaps added in a common floodmap, shown in the following Figure 11. The measurement demonstrates good small crystal separation capabilities of the sensor. Again, no other corrections except the non-linearity correction were applied to the data.

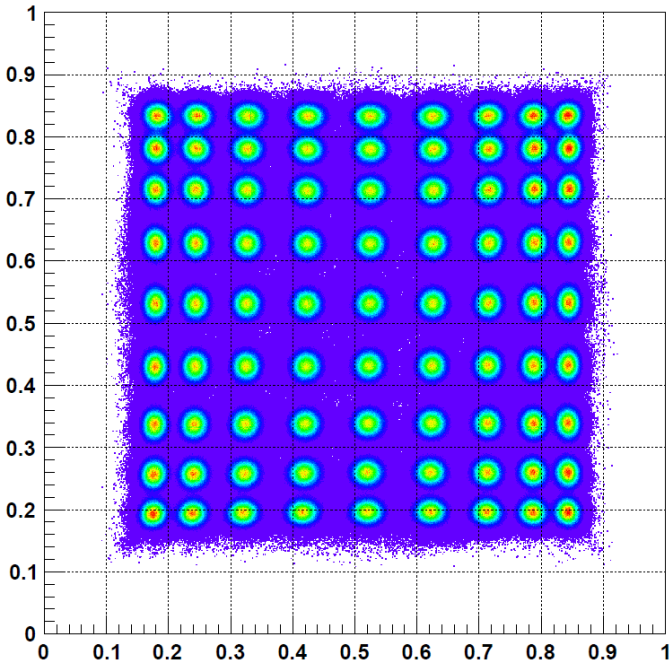

Fig. 11. Synthetic floodmap based on a picosecond-pulsed laser beam measurement on a XY stage at 1600 photons per position. The stage step width was 500µm between adjacent positions.

IV. Applications

A. Single Photon Imager

For some applications, it may be useful to obtain the image of the average light intensity spread over the sensor. This may include, for example, the verification or fine-tuning of a light guide design. This measurement can be readily realized with relatively low effort using the methods implemented for the acquisition of the dark count rate map of the Digital Silicon Photomultiplier. In this case, the diodes are selected one-by-one and the dark count rate is measured for each diode separately, resulting in the analogon to the dark image of a CMOS or CCD image sensor. Using light sources, the same method can be used without alteration to acquire the average image of the light spread. The usual correction methods like dark image subtraction, sensitivity normalization etc. can be applied to improve image quality and quantification.

In addition to these already known corrections, further suppression of the image noise can be achieved using a coincidence setup. In this case, a reference sensor is used to filter events related to gamma detections, while the device-

under-test sensor is used to measure the number of optical photons seen by the selected diode. Again, a consecutive measurement of all diodes results in the map of the average light spread over the sensor, as shown in Fig. 12 for an exemplary arrangement of small crystals glued directly to the dSiPM surface. Electronic and/or mechanical collimation can be used to select a single crystal in an array.

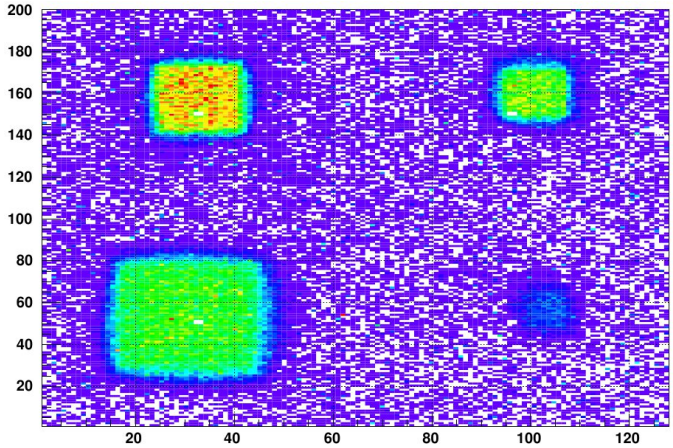

Fig. 12. Coincidence image of the light emitted by a configuration of small crystals glued directly to the sensor surface. The size of the smallest crystal is 0.5x0.5x10mm³.

B. Čerenkov Light Detection

We successfully tested the technology demonstrator as a sensor for Čerenkov light. The test setup shown in Fig. 13 was developed by the team of Prof. Düren at Gießen University, Germany and tested at Philips Digital Photon Counting in Aachen using a picosecond-pulsed laser beam [6].

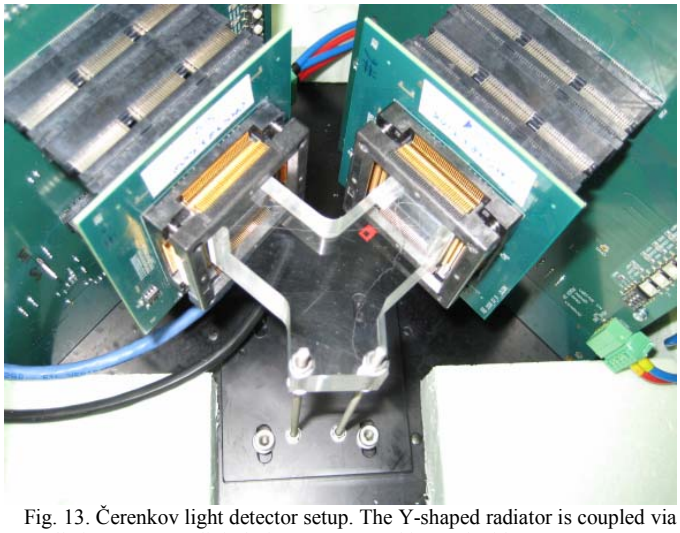

Fig. 13. Čerenkov light detector setup. The Y-shaped radiator is coupled via a small air gap to two digital SiPMs connected in a coincidence setup.

For the beam test, the Y-shaped Čerenkov radiator made of acrylic glass was coupled via approximately 1 mm air gap to two DLD8K demonstrator chips described in [3] connected in coincidence. The measurements were carried out using 120GeV protons from the SPS test beam at CERN. The test setup was operated in first-photon trigger mode and all events have been validated. The setup temperature of 3°C was controlled by a thermoelectric cooler and 2% of the diodes with the highest dark counts have been disabled to further reduce the dark count rate of the sensors. The measured dark count rates for both sensors were in the range of 500kHz. Additionally, an external gate signal was used to reduce the number of random coincidences due to the low beam duty cycle of only 16%, to reduce the data file size. Measurement times ranged from few minutes to several hours. Coincidence resolving time of $\sigma = 86$ps was measured for both sensors (Fig. 14), resulting in $\sigma = 61$ps per sensor.

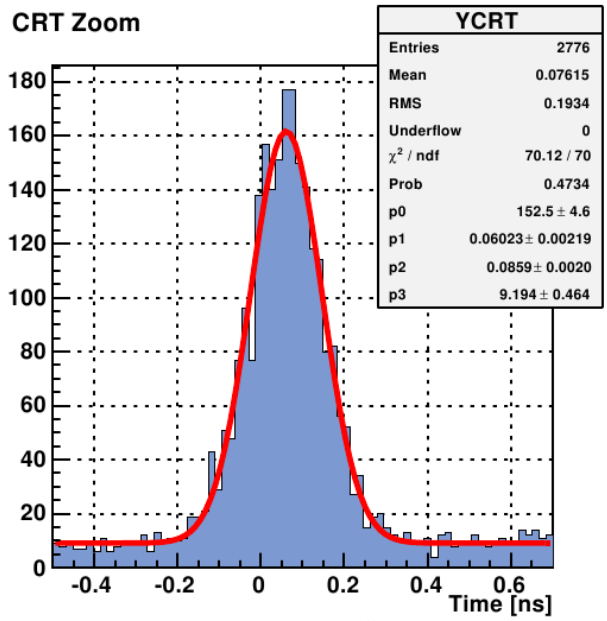

Fig. 14. Coincidence time resolution of the Čerenkov light detector.

As stated previously, the skew in the trigger network is currently the major contributor to the time resolution for single photons. Re-balancing and fine-tuning of the trigger network will make it possible to improve the time resolution of the sensor to 30ps – 40ps at the single-photon level.

V. Summary

We developed a fully integrated digital implementation of the Silicon Photomultiplier. The device is manufactured in a high-volume CMOS process and includes single photon avalanche photodiodes, the detection and readout circuits as well as two time-to-digital converter and associated controllers on the same substrate. The sensor is capable of detecting single photons and scintillator pulses as well as identifying scintillator crystals in arrays with less than 1 mm crystal pitch.

The sensor is designed with large area applications in mind. It provides a standard JTAG interface for configuration and two 100MHz serial data output links. The reference clock and test signals can be supplied either in single-ended or differential mode. Detector tiles based on the sensor have been developed and tested (see [5]) and a modular and scalable readout system for the sensors is currently under development.

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