PHILIPS

sense and simplicity

Digital Silicon Photomultiplier

System Architecture and Performance Evaluation

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Philips Digital Photon Counting
Digital SiPM – New Type of Silicon Photomultiplier

**Analog SiPM**
- Cells connected to common readout
- Analog sum of charge pulses
- Analog output signal

**Digital SiPM**
- Each diode is a digital switch
- Digital sum of detected photons
- Digital data output

[TDC and photon counter]

*Digital output of*
- Number of photons
- Time-stamp

[www.hamamatsu.com]
Digital SiPM – Cell Electronics

- Cell electronics area: 120µm²
- 25 transistors including 6T SRAM
- ~6% of total cell area
- Modified 0.18µm 5M CMOS
- Foundry: NXP Nijmegen
Digital SiPM – Sensor Architecture

- Operating frequency: 200MHz
- 2 x TDC (bin width 23ps, 9bit)
- Configurable trigger network
- Validation logic to reduce sensor dead time due to dark counts
- JTAG for configuration and scan test
- Electrical trigger input for test and TDC calibration
Digital SiPM – Sensor Family

DLD8K Demonstrator (2009):

- 8192 cells
- Integrated TDC
- On-chip inhibit memory controller
- External FPGA controller
- 160 bond wires

DLS 6400-22 digital SiPM (2010):

- 25600 cells
- 2 TDCs, controller, data buffers
- JTAG for configuration & test
- 48 bond wires
Digital SiPM – Dark Counts

Control over individual SPADs enables detailed device characterization

- Over 90% good diodes (dark count rate close to average)
- Typical dark count rate at 20°C and 3.3V excess voltage: ~150cps / diode
- Low dark counts (~1-2cps) per diode at -40°C
Digital SiPM – Photon Detection Efficiency

- Peak PDE >30% at 430nm and 3.3V excess voltage
- No anti-reflective coating used, optical coupling not optimized
- Needs independent verification

Effective PDE:
- LYSO(Ce): 25.9%
- CsI(Na): 23.7%
- CsI(Tl): 20.5%
- NaI(Tl): 24.2%
- BGO: 24.2%
- LaBr₃(Ce): 9.6%
Direct measurement using one 'bad' diode as light generator:

- Acquire dark count map around the light source for corrections
- Activate light source **and** test diode simultaneously:
  - Events with 1 photon are dark counts
  - Events with 2 photons are either randoms or optical crosstalk
- Use the dark count map to correct for randoms

Typical total optical crosstalk in a 5x5 neighborhood: 7% - 9%
Digital SiPM – Temperature Sensitivity

ps-laser trigger, 2100 photons/pulse, 24ps FWHM timing resolution

- PDE drift: 0.33% K\(^{-1}\)
- TDC drift: 15.3ps K\(^{-1}\)
- PDE drift compensation by adapting the bias voltage
- TDC re-calibration using electrical trigger
Digital SiPM – Photon And Time Resolution

- Sensor triggered by attenuated laser pulses at first photon level
- Laser pulse width: 36ps FWHM, $\lambda = 410$nm
- Contribution to time resolution (FWHM):
  
  **SPAD**: 54ps, trigger network: 110ps, TDC: 20ps

- Trigger network skew currently limits the timing resolution
Digital SiPM – Scintillator Measurements

- 3 x 3 x 5 mm³ LYSO in coincidence, Na-22 source
- Time resolution in coincidence: 153ps FWHM
- Energy resolution (excluding escape peak): 10.7%
- Excess voltage 3.3V, 98.5% active cells
- Room temperature (31°C board temperature, not stabilized)
New Experimental Design (DLS 3200-22):

- 3200 cells per pixel, 12800 cells per sensor
- 59.4µm x 64µm cell size, 78% area efficiency (incl. electronics)
- Based on (and compatible to) DLS 6400-22 sensor
Digital SiPM – DLS 3200-22 Dark Count Rate

- Dark count rate at 20°C, 3.3V excess voltage
- Average dark count rate ~ 550cps per SPAD
- Scales with SPAD sensitive area (2954µm² vs. 783µm² in DLD8K)
Digital SiPM – DLS 3200-22 Optical Crosstalk

- Optical crosstalk ~18% due to higher diode capacitance (factor ~2.8)
- Linear dependence on excess voltage (as expected)
- Has to be taken into account in saturation correction
Digital SiPM – DLS 3200-22 Energy Resolution

- 4 x 4 x 22 mm³ LYSO crystal
- Vikuiti reflector
- Attached with Meltmount
- Na-22 source
Digital SiPM – DLS 3200-22 Energy Resolution

- 3.3V excess voltage, 20°C
- 99% active cells
- Non-linearity correction
- Optical crosstalk included [Burr et al.]
- dE/E = 9.2%
Digital SiPM – DLS 3200-22 Saturation Correction

Saturation correction including optical crosstalk model [Burr et al., 2007]:

Simple saturation correction neglecting optical crosstalk:

- Optical crosstalk seems to limit the energy resolution
Digital SiPM – Tiles

• 4 x 4 sensor array
• 8 x 8 pixels
• 4-sides tileable
• see also Poster: PI-68
Digital SiPM – Small Crystal Identification

• Laser measurements on a 0.5mm grid
• Best case (no scatter, no light guide)
• ~1600 photons per laser pulse
Digital SiPM – Small Crystal Identification

- Array of 30 x 30 LYSO crystals
- Crystal size: 1 x 1 x 10mm³
- Coupled via light guide to one digital SiPM tile (4 x 4 dies)
- Data plotted in log scale
- Strong floodmap compression close to tile edge due to missing neighbor tiles

P. Düppenbecker, Philips Research
Digital SiPM – Čerenkov Light Detection

- PMMA radiator coupled via air gap to two dSiPMs (DLD8K) in coincidence
- Box isolated and temperature-controlled with a TEC to 2 – 3°C
- Cooperation between Giessen University (Prof. Düren) and Philips DPC
- First measurements at CERN SPS: $\sigma = 60.7\text{ps}$
Summary

• Digital SiPM implemented in a high-volume CMOS process
• Configurable architecture, individual control of each SPAD
• Two-sides tileable sensor design
• Tiles of 4 x 4 sensors developed to simplify system integration
  (see also poster presentation PI-68 by C. Degenhardt)
• New design with improved fill factor of 78% currently being tested

The author would like to thank Dr. Hein Valk of NXP Semiconductors for his support and excellent cooperation during the process development
Visit us at booth 5 or www.philips.com/digitalphotoncounting
Digital SiPM – State Machine

- 200MHz (5ns) system clock
- Variable light collection time up to 20µs
- 20ns min. dark count recovery
- dark counts => sensor dead-time
- data output parallel to the acquisition of the next event (no dead time)
- Trigger at 1, ≥2, ≥3 and ≥4 photons
- Validate at ≥4 ... ≥64 photons (possible to bypass event validation completely)
Digital SiPM – Sensor Architecture

- JTAG in
- data out
- LVCMOS clock & sync
- JTAG out
- LVDS clock & sync

- Main controller
- TDC
- JTAG controller
- Trigger logic
- Pixel controllers
- Sub-pixel
Digital SiPM – Trigger Logic

- Each sub-pixel triggers at first photon
- Sub-pixel trigger can be OR-ed or AND-ed to generate probabilistic trigger thresholds
- Higher trigger threshold decreases system dead-time at high dark count rates at the cost of time resolution
Digital SiPM – Trigger Network Skew

- Diodes activated one-by-one and triggered by a divergent ps-laser pulse.
- Many photons per diode&pulse → negligible avalanche spread uncertainty.
- Laser trigger&pulse spread and TDC resolutions are included in the final $\sigma$. 
Digital SiPM – Time-to-Digital Converter

- Two identical 9 bit TDCs running with 180° phase-shifted clocks
- 100MHz reference clock generated from 200MHz system clock
- Each TDC has ~0.5ns wide 'blind spot' close to clock edge → bin 0
- Two-phase clock guarantees at least one valid TDC value for any event
- For ~90% of the events, both TDC values can be used to increase accuracy
- TDC calibration using dark counts or randomly distributed events
Digital SiPM – Time-to-Digital Converter

- Average TDC bin width $23 \pm 2.8\text{ps}$
- Non-linearity corrected by look-up tables inside the readout FPGA
- Online correction for TDC drift due to temperature and voltage variation
- Periodic TDC calibration test using external (SYNC) signal
Digital SiPM – Trigger Network Skew

- Chip illuminated by divergent picosecond laser beam
- Laser trigger synchronized to the reference clock
- All diodes measured sequentially
- 10000 events captured and time stamp histogram fitted with a Gaussian
- Gaussian mean → delay of the selected trigger path
- Average trigger network delay subtracted from the data